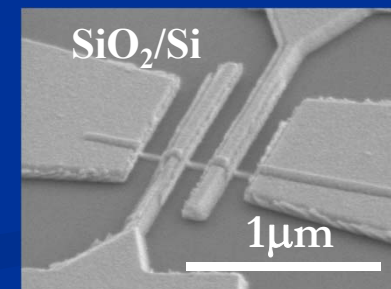
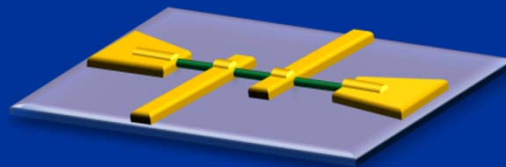


無機・有機融合型ヘテロナノワイヤの ネットワーク構造体を用いた超Tbit 級 不揮発性メモリ素子の研究開発



柳田 剛、谷口正輝

大阪大学 産業科学研究所

Backgrounds –why resistive switching?–

Resistive switching memory effects

ReRAM, Memristor

IMEC



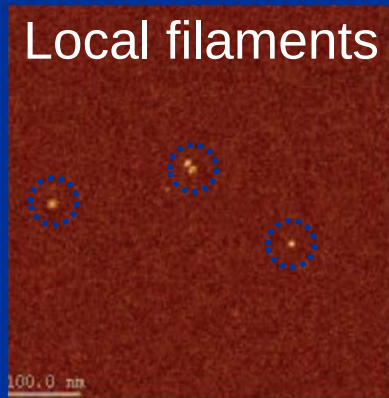
SHARP



SONY

Nature Materials (2007)

Local filaments

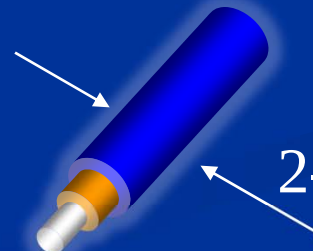
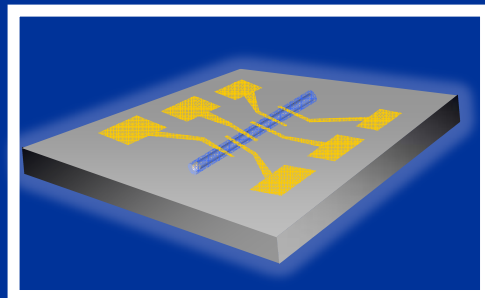


Oxides

What is happening at nanoscale?



Single Oxide Nanowire Device



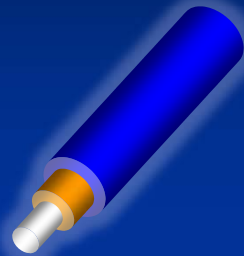
2-10nm

Nano-scale Mechanism

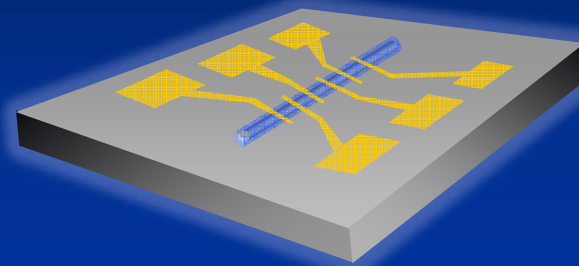
Nano-Device Applications

We want to extract the internal RS events!!

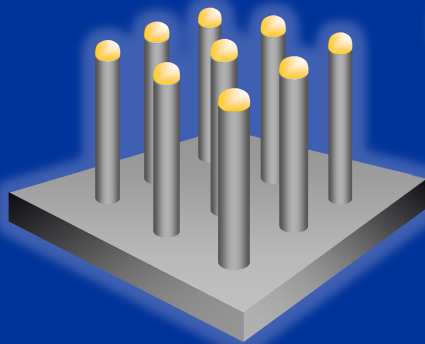
Our Strategy



Heterostructured
Oxide Nanowires

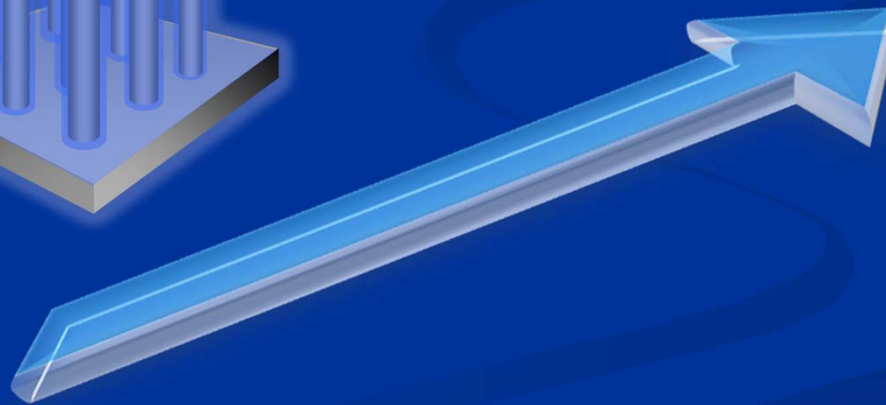
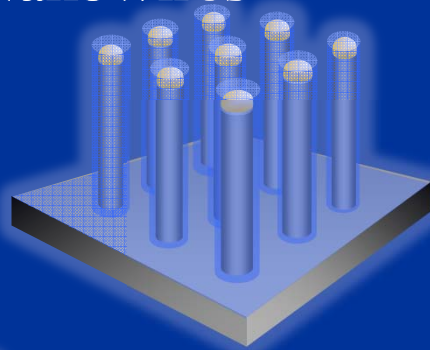


Single oxide nanowire device
Extraction of resistive switching
properties

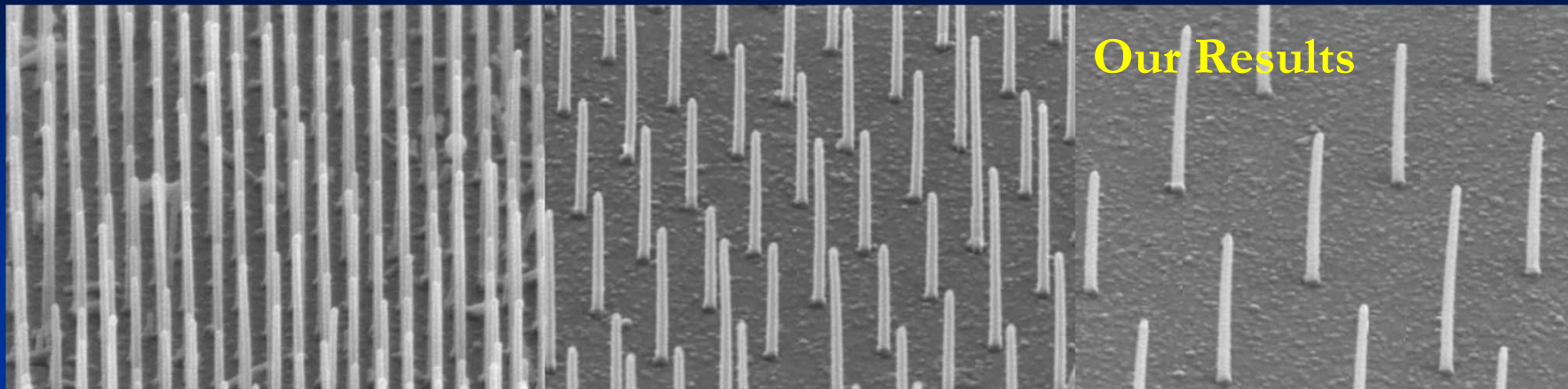


1D Oxide Nanowire

Vapor-Liquid-Solid (VLS) growth



How can we fabricate nanowires?

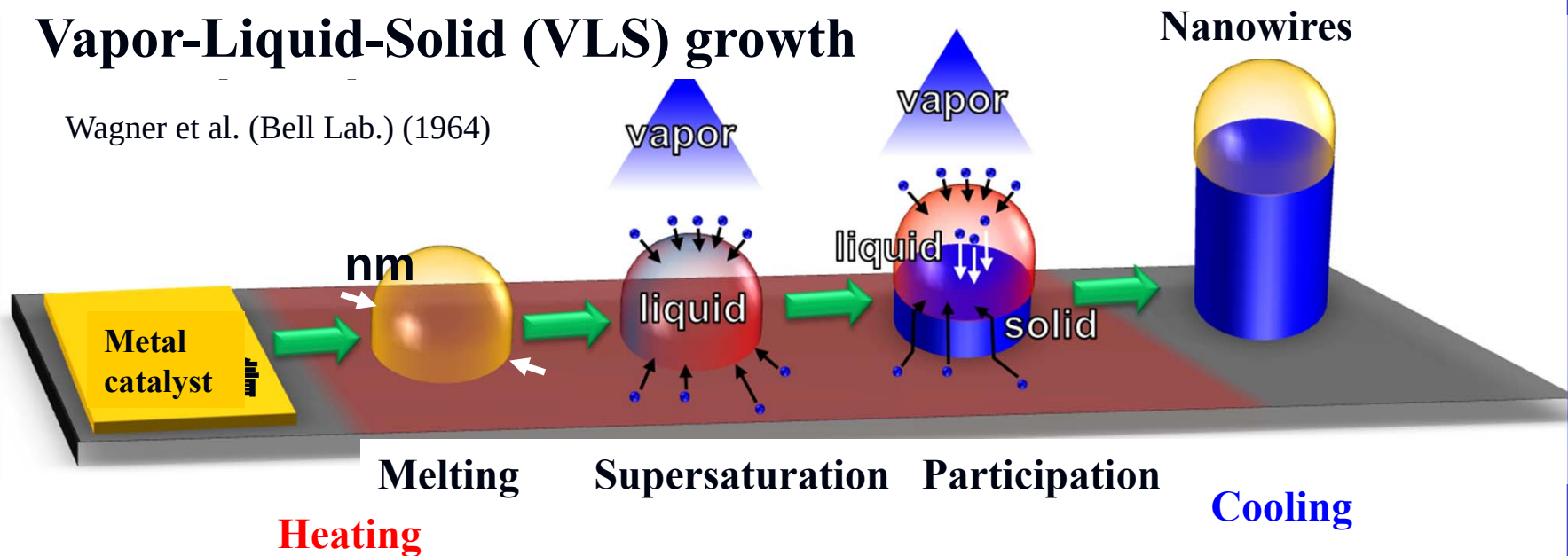


Our Results

method

Vapor-Liquid-Solid (VLS) growth

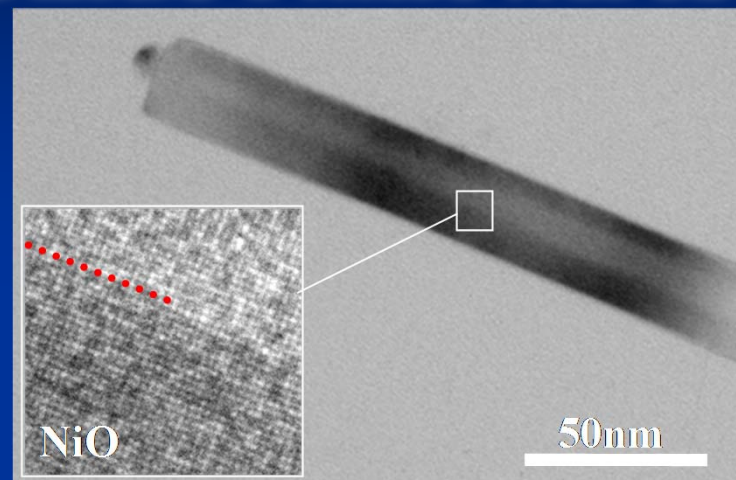
Wagner et al. (Bell Lab.) (1964)



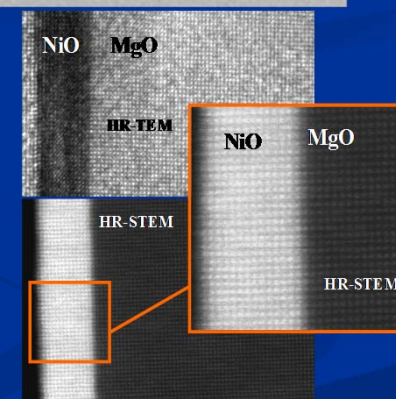
Well-defined Single Crystalline Heterostructured Oxide Nanowires



Appl. Phys. Lett. 90, 233103 (2007)
Appl. Phys. Lett. 91, 061502 (2007)
Appl. Phys. Lett. 93, 153103 (2008)
Appl. Phys. Lett. 97, 016101 (2010)
Phys. Rev. E, 82, 011605 (2010)
Phys. Rev. E, 83, 061606 (2011)

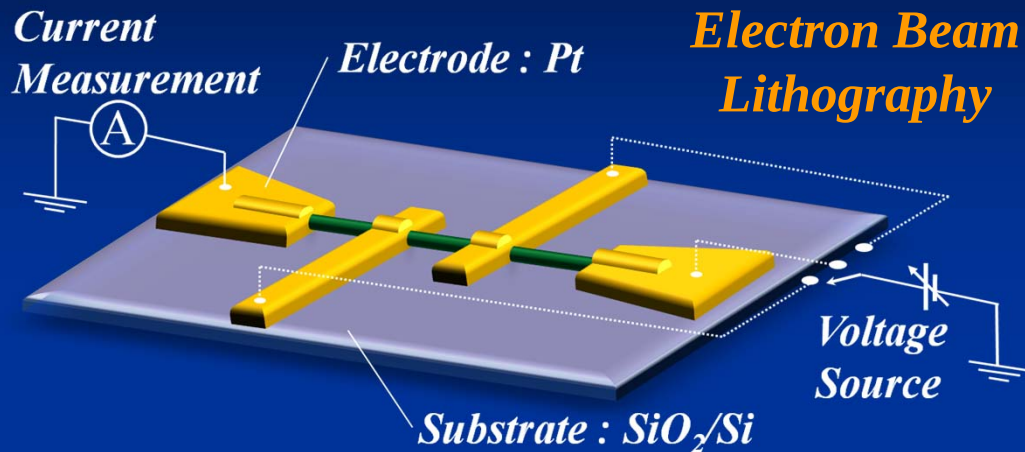


J. Am. Chem. Soc. 130, 5378 (2008)
Appl. Phys. Lett. 92, 173119 (2008)
Appl. Phys. Lett., 95, 133110 (2009)
J. Am. Chem. Soc. 131, 3434 (2009)
J. Am. Chem. Soc., 132, 6634 (2010)
J. Am. Chem. Soc., 133, 12482 (2011)
Nano Lett., 10, 1359 (2010)
Nano Lett., 11, 2114 (2011)



We can fabricate diverse “Functional” oxide nanowires by using this method!!

“Single Nanowire” Device



Cross-sectional area of single nanowire devices

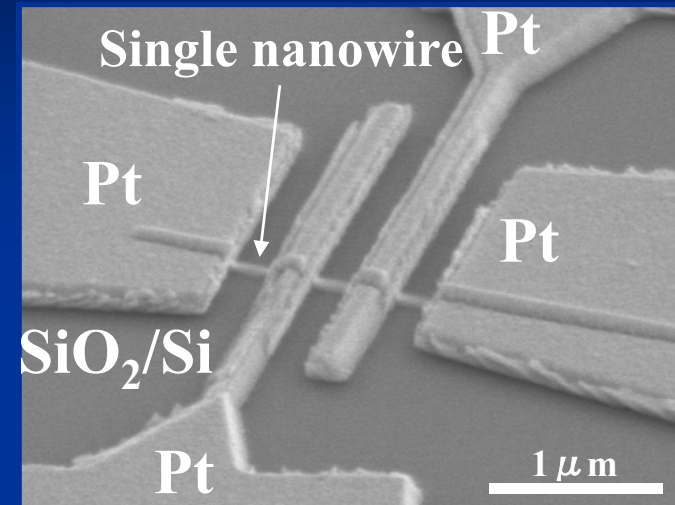
$$< \sim 10^2 (\text{nm}^2)$$

Used Nanowires *p*-type

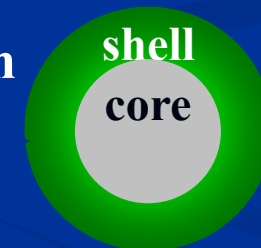
NiO heterostructured nanowires

CoO_x heterostructured nanowires

SEM image



shell : ~5nm



n-type → oxygen vacancies

p-type → ? ? (cation? oxygen?)

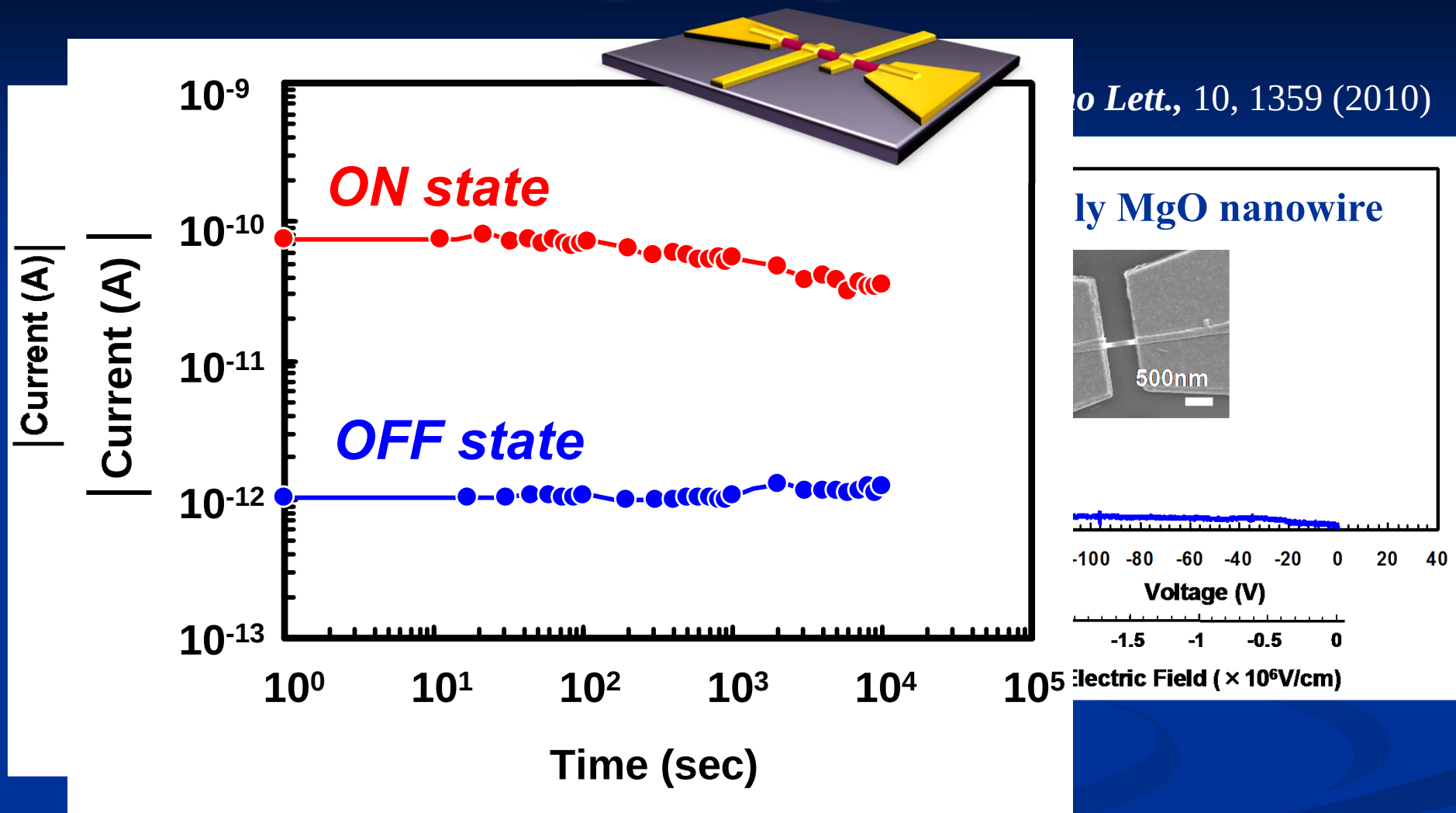
What we want to clarify are:

- **Can we observe the resistive switching in a single oxide nanowire device $<10\text{nm}$?**

(Stability? Multistate? at ultra small nanoscale)

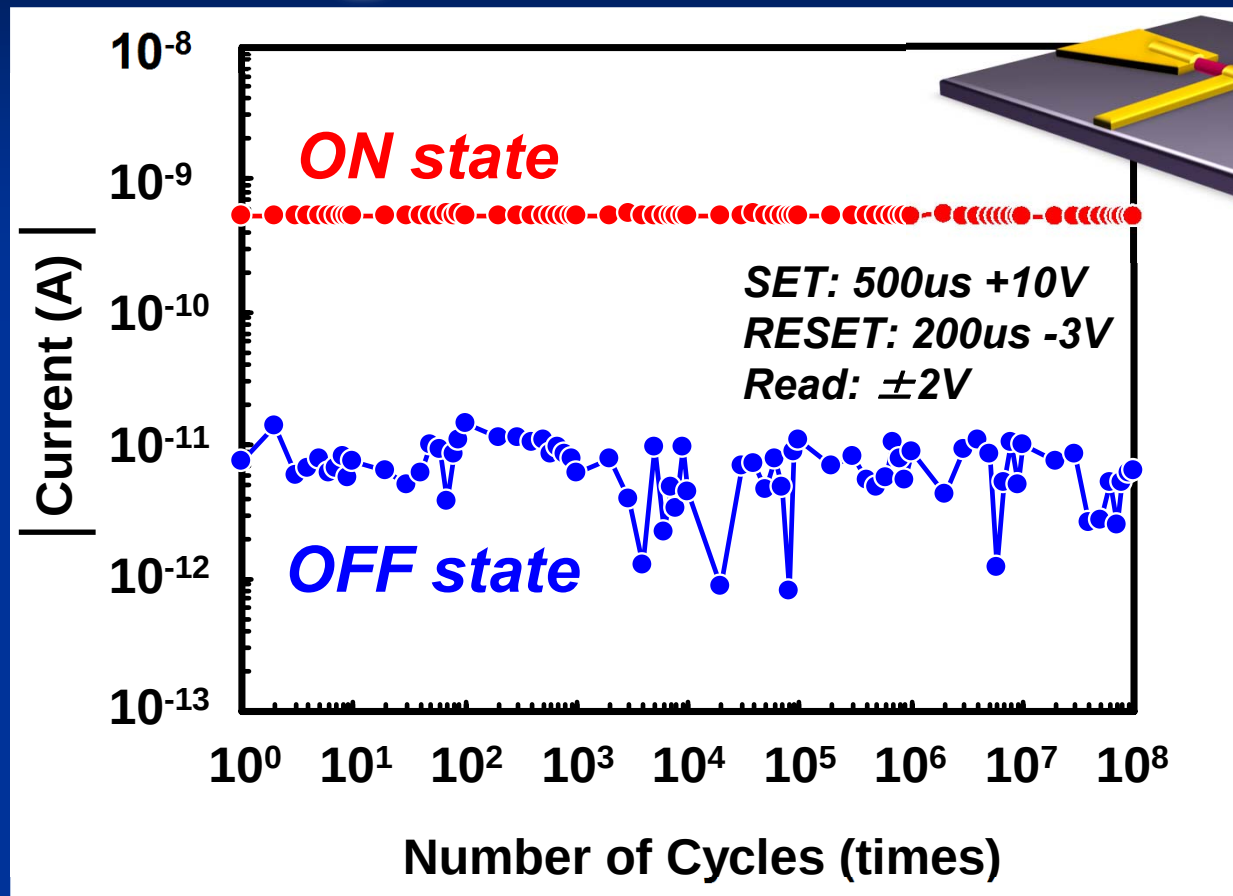
- **What is the conduction nature of resistive switching in p-type oxides?**

Resistive Switching in Single Nanowire Device



1. Resistive Switching effects < 10nm scale
2. 100pA-1 μ A current range operation

Stable Memory Operation –Endurance – in Single Nanowire Device



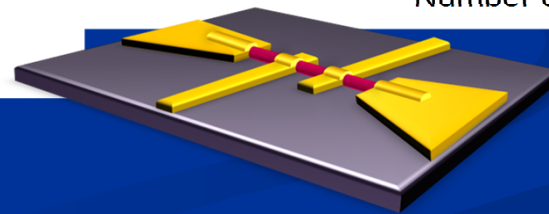
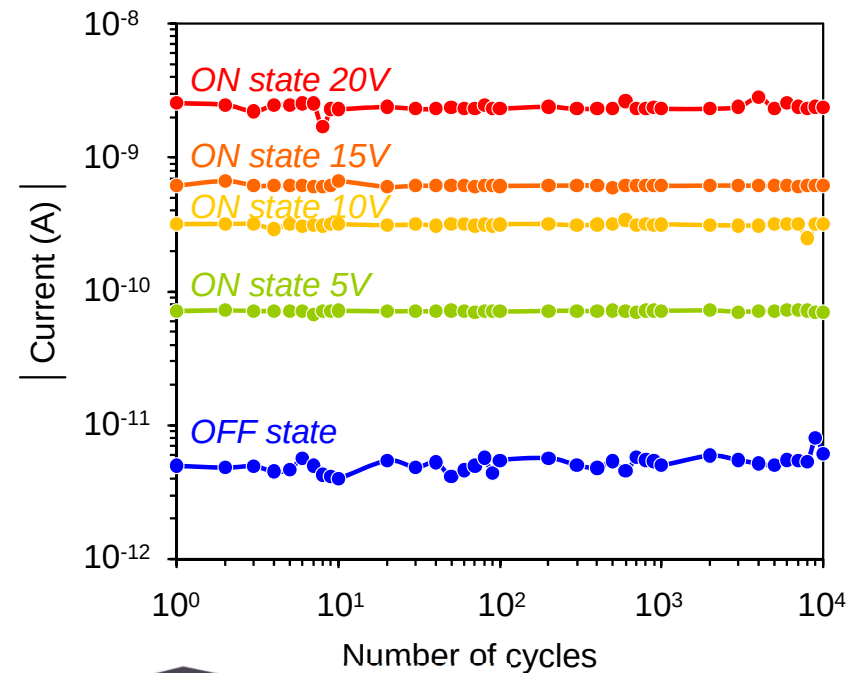
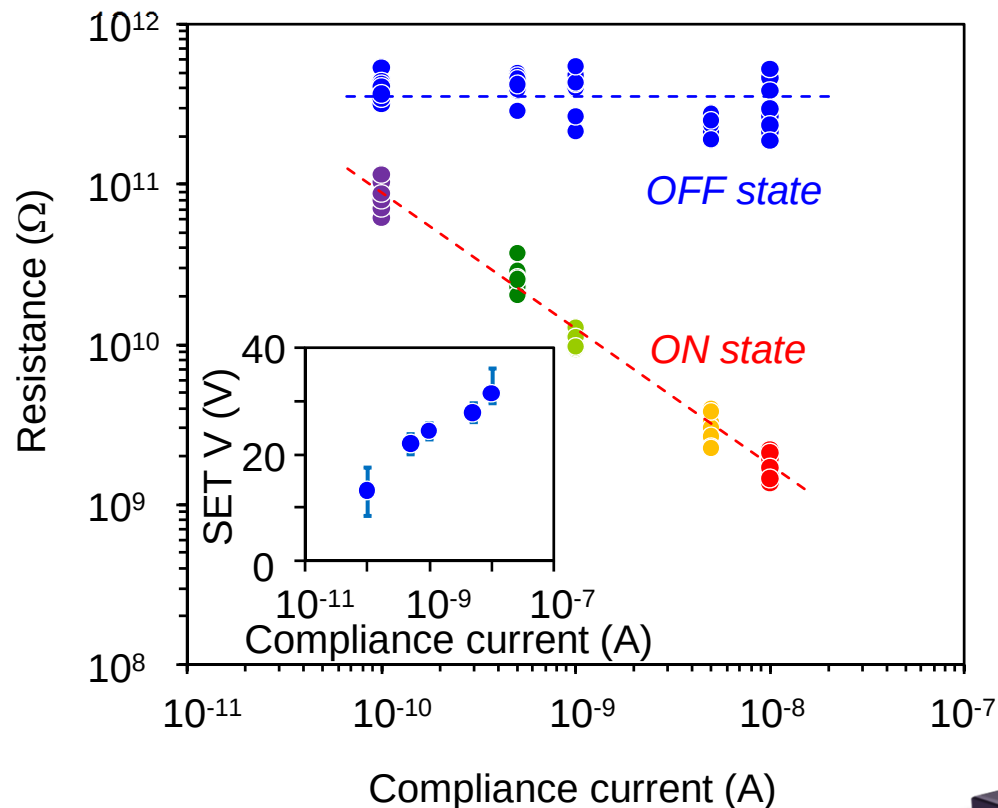
Nano Lett., 10,
1359 (2010)

The endurance, at least up to **10⁸**, at **10 nm scale**

Top record at this scale, **Nano-ReRAM** is promising!

Stable “Multistate” Memory Operation in Single Nanowire Device

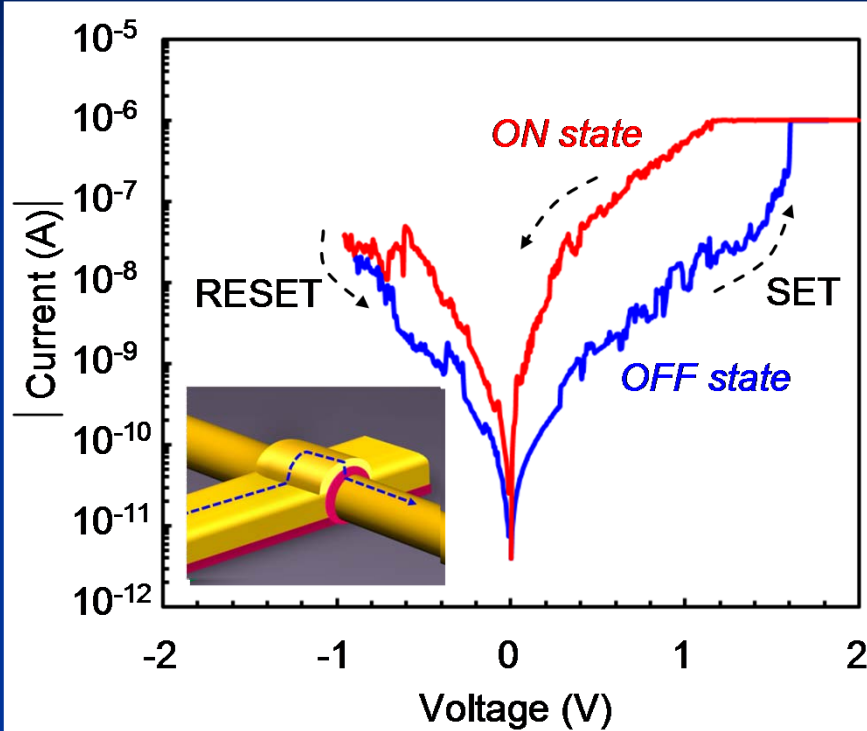
Nano Lett., 10, 1359 (2010)



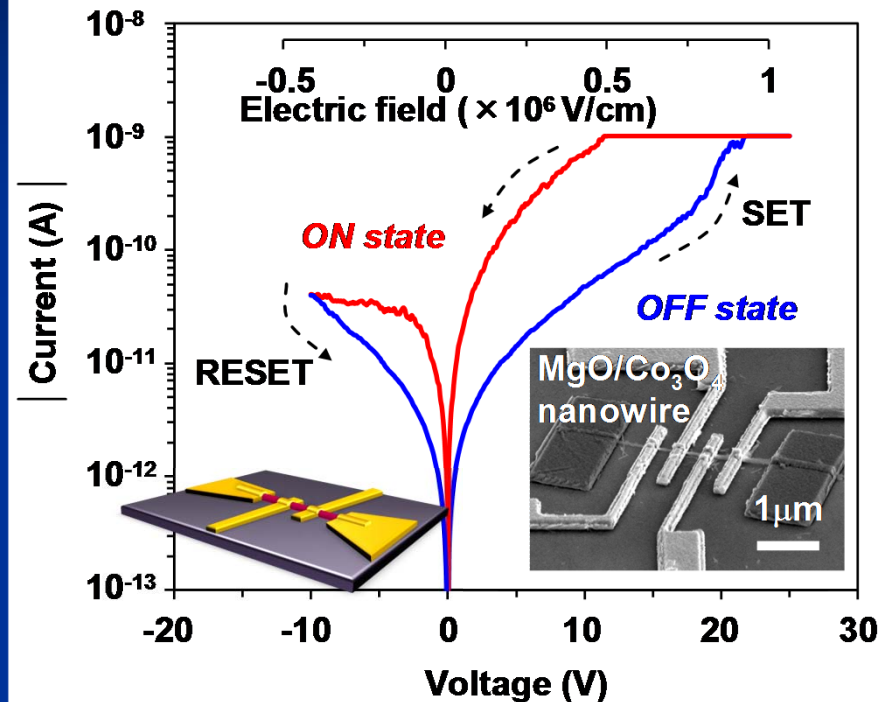
The **multistate operation** is feasible at 10nm.

Nanowire Cross-Point Devices

I-V characteristics of cross-point device



I-V characteristics of nanowire device



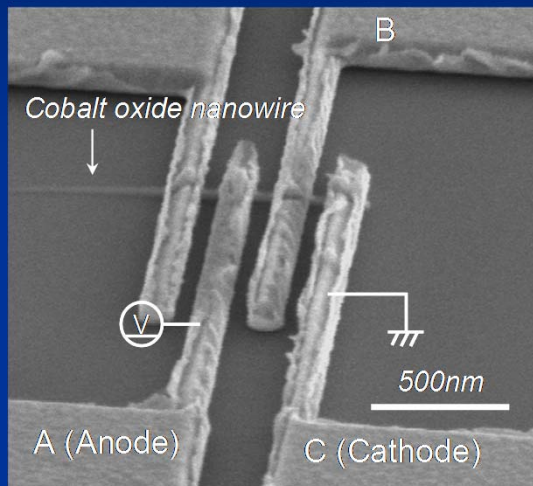
	Voltage	Electric Field Intensity	Power
Cross-Point nanowire device	1-2V	$0.3-0.6 \times 10^6 \text{ V/cm}$	$\sim 10^{-7} \text{ W}$
Nanowire device	15-40V	$0.6-1.6 \times 10^6 \text{ V/cm}$	$\sim 10^{-8}-10^{-6} \text{ W}$
Reported Thin film device	1-5V	$0.3-1.6 \times 10^6 \text{ V/cm}$	$\sim 10^{-2}-10^{-3} \text{ W}$

Where is the switching location?

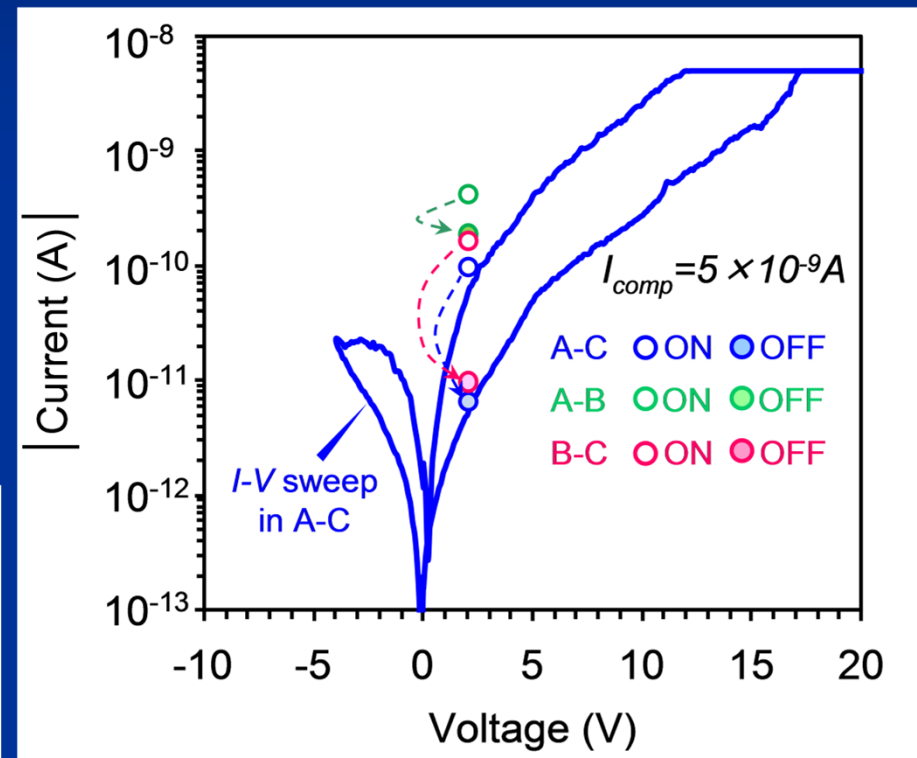
Where is active switching location?

Nano Lett., 11, 2114 (2011).

Detection of local resistance change



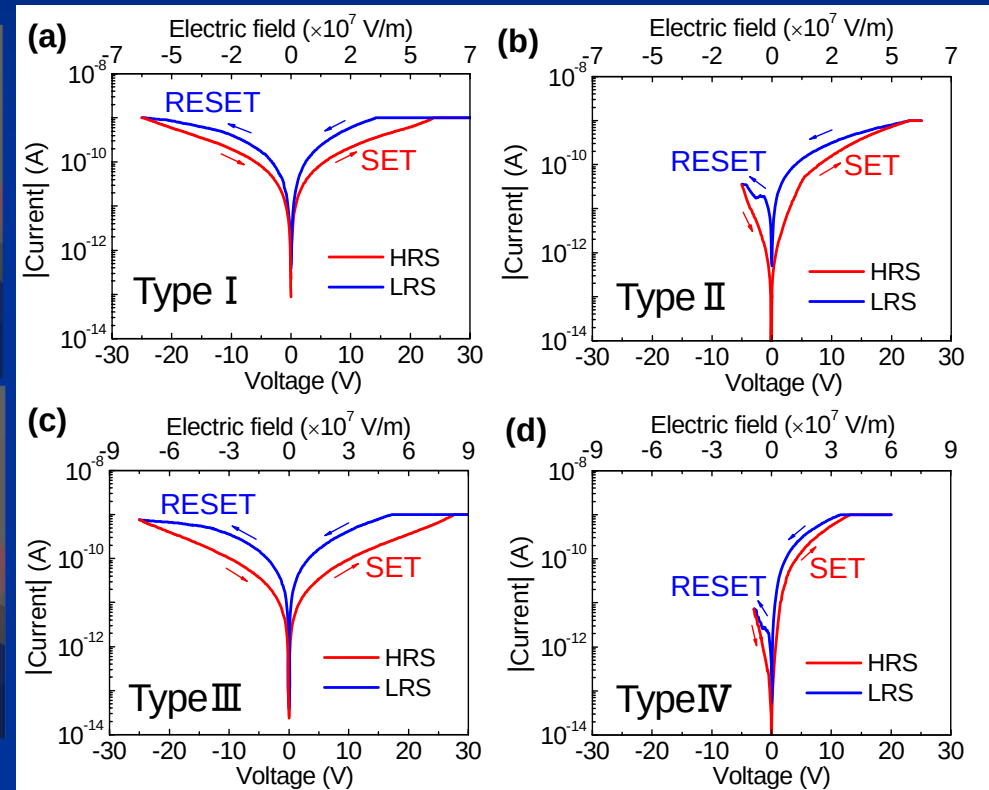
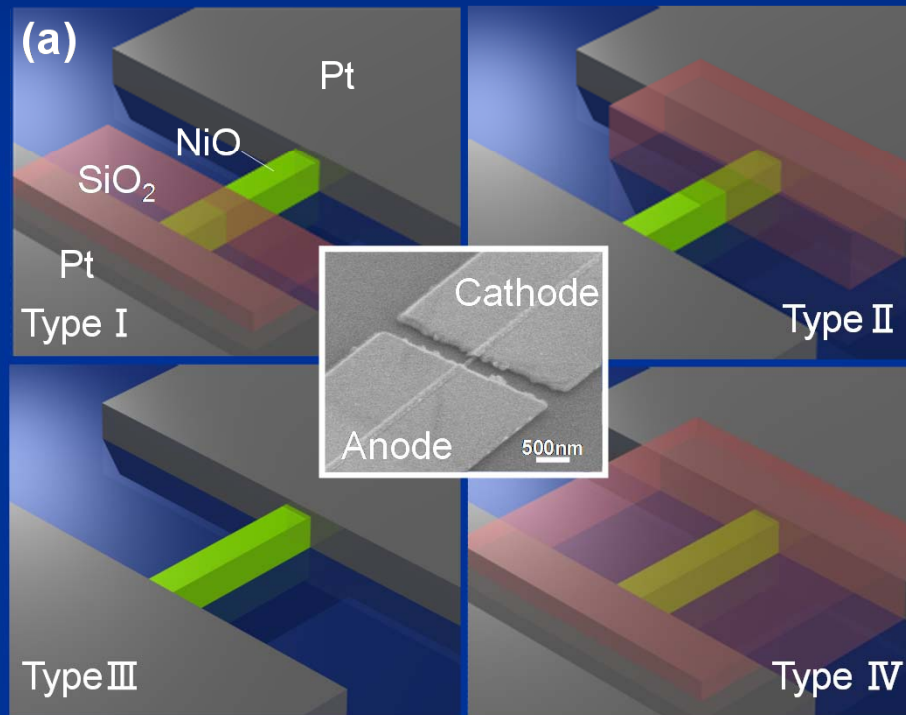
measured area	ON state resistance (Ω)	OFF state resistance (Ω)	ON/OFF ratio
A(anode)-C(cathode)	2.06×10^{10}	3.02×10^{11}	14.7
A-B(anode side)	4.74×10^9	1.06×10^{10}	2.2
B-C(cathode side)	1.20×10^{10}	2.05×10^{11}	17.1



Resistive switching occurs near **“Cathode”** in the case of p-type oxides (NiO and CoOx)!!

Where is the switching location?

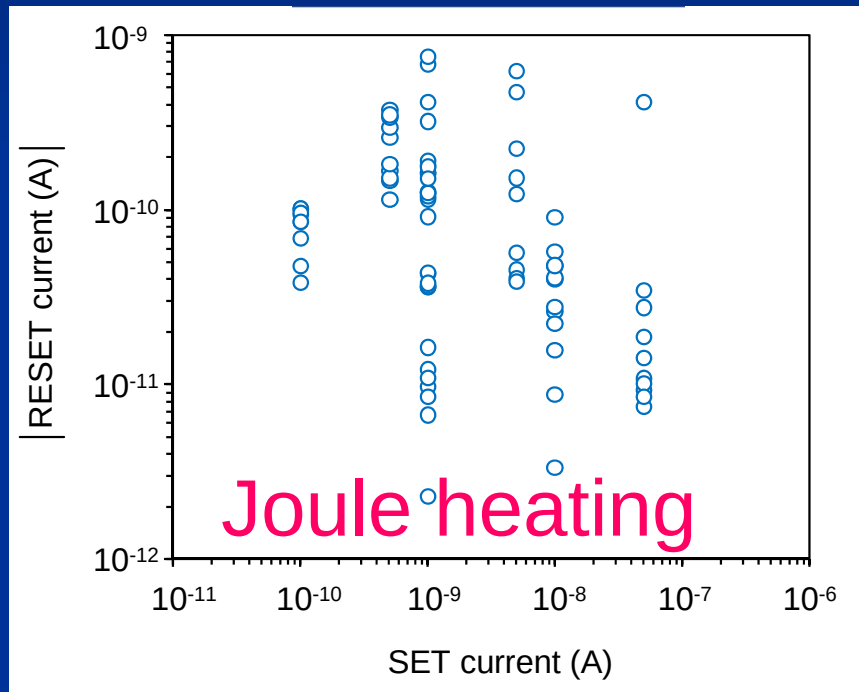
J. Am. Chem. Soc., 133, 12482(2011)



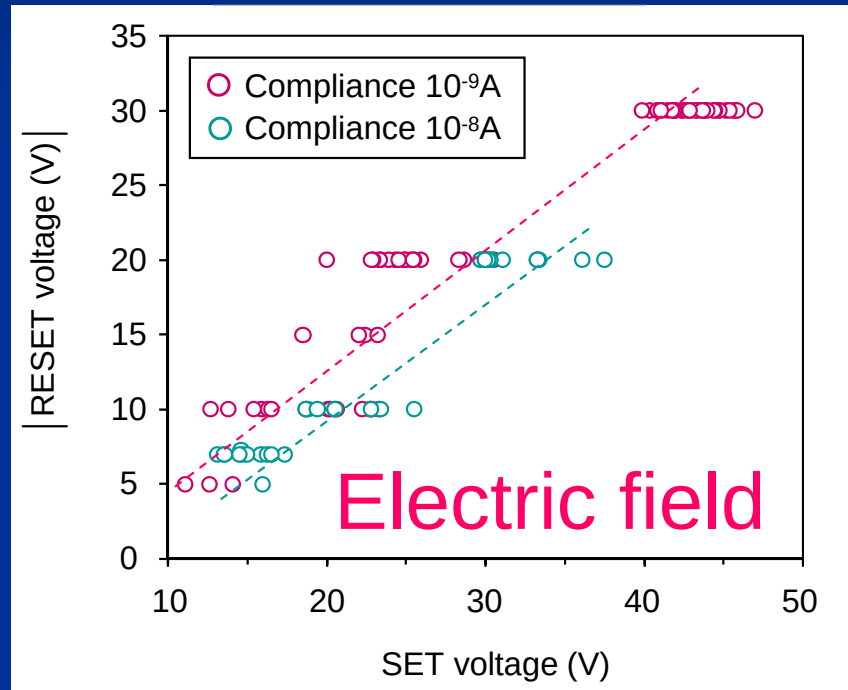
Resistive switching occurs near “**Cathode**” in the case of p-type oxides (NiO)!!

What is the nature of conduction?

I - I plot



V - V plot



Previous: Unknown



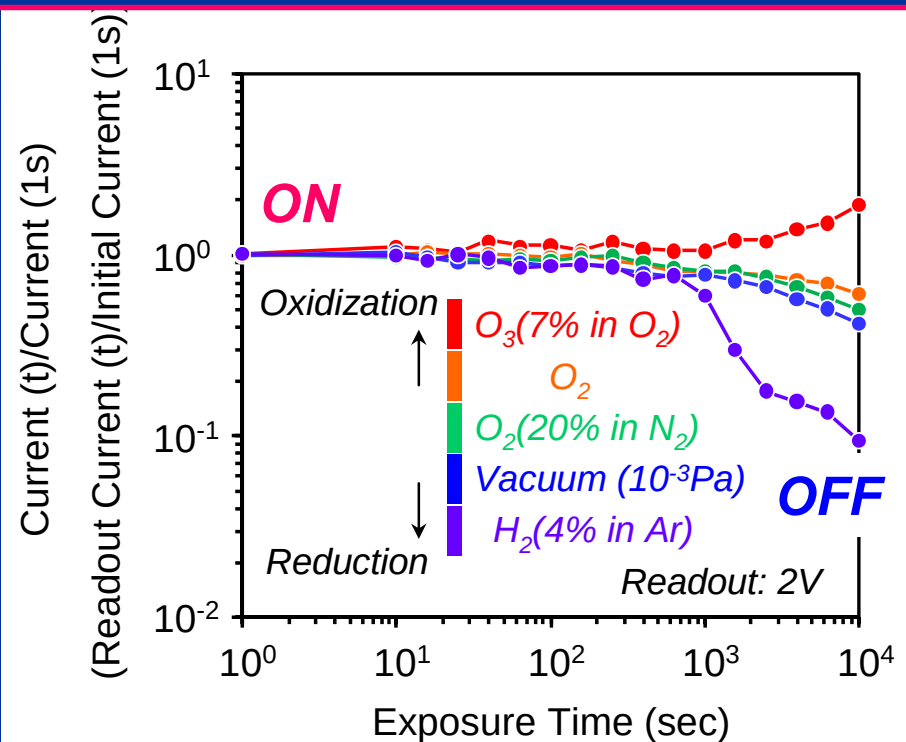
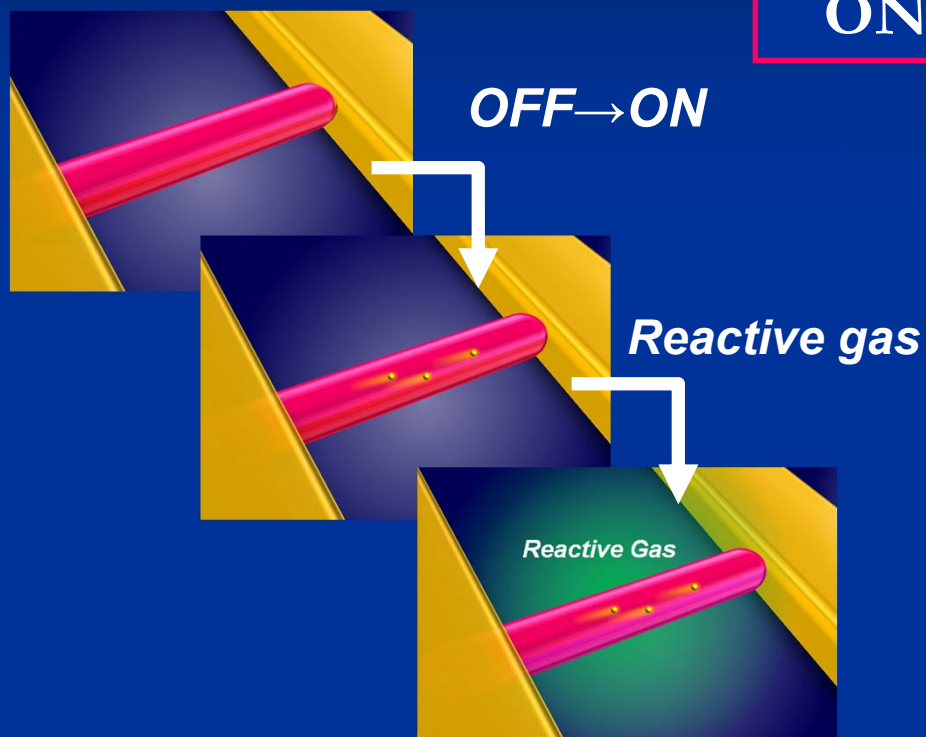
Electric field induced memory effect

Nano Lett., 11, 2114 (2011).

What is the nature of conduction?

Data retention in various atmospheres

ON: Oxidization OFF: Reduction??



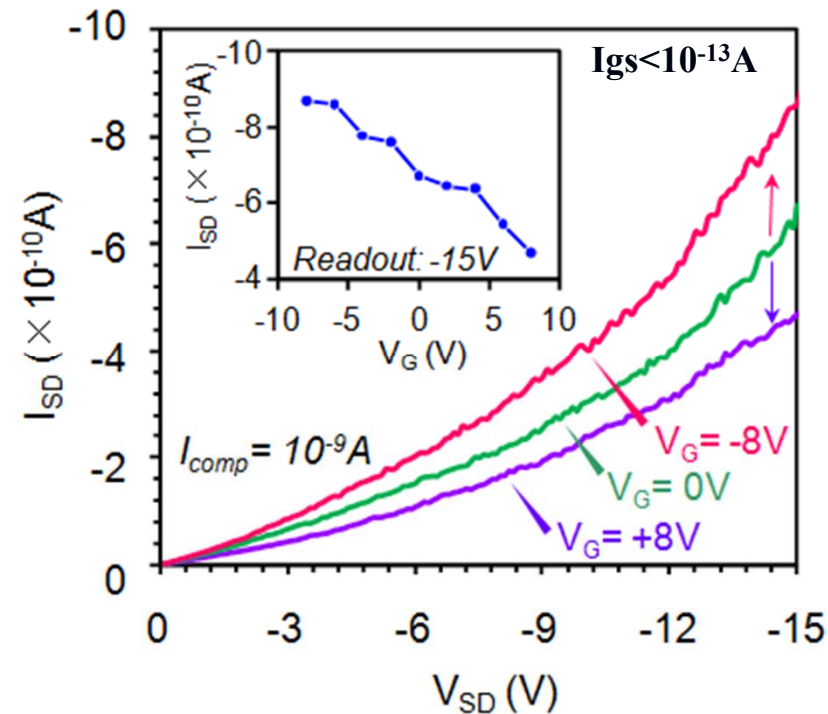
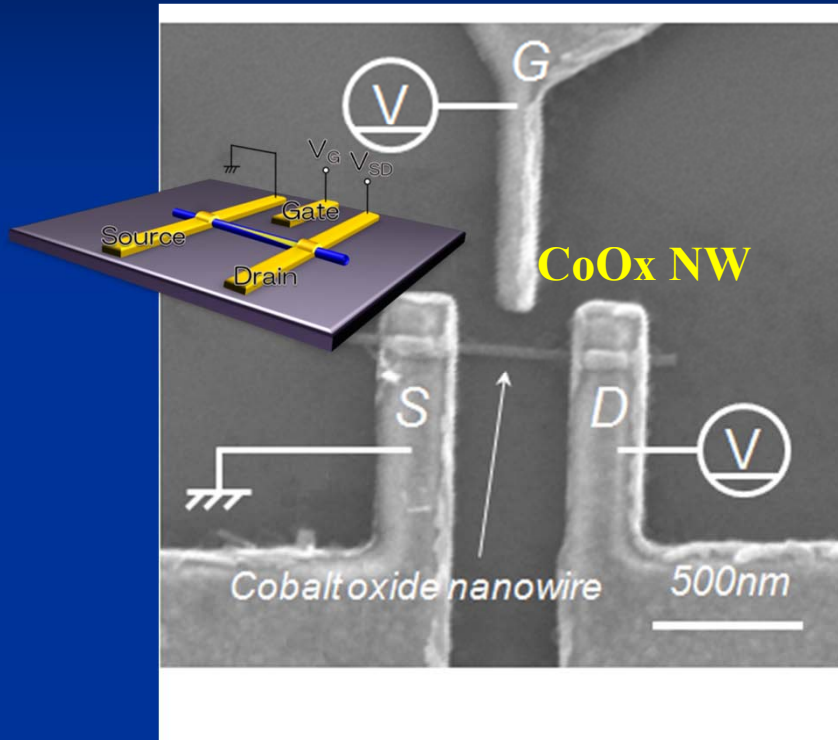
Nano Lett., 11, 2114 (2011).

Previous: Redox? (Lack of crucial data)

Resistance change by redox

What is the carrier type ?

After SET process,



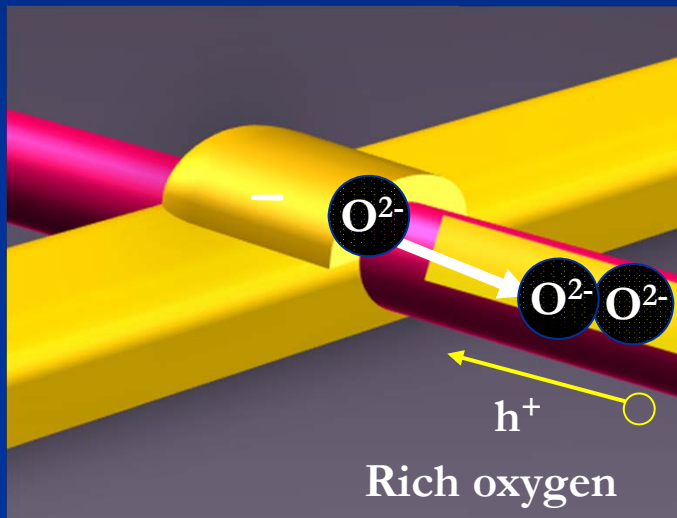
Nano Lett., 11, 2114 (2011).

FET measurements demonstrated
***p*-type channel in NiO and CoOx!**

Mechanisms in p-type oxides

Mechanism of memristive switching

Highlighted in Nature asia-pacific (13 June 2011)



-Switching near Cathode

-OFF: Reduction ON: Oxidization

Intrinsic nature of memristor was found.



The image is a screenshot of a news article from Nature Asia-Pacific. The header includes the "npg" logo and the text "nature asia-pacific Highlighting the best research from the Asia-Pacific". Below the header, it says "NPG Asia Materials featured highlight | doi:10.1038/asiamat.2011.89 Published online 13 June 2011". The main title of the article is "Resistive memory: Total exposure". The sub-headline reads: "Resistive memory built with exposed, planar nanowires provides insights into resistive switching." The main text describes the current standard for non-volatile 'flash' memory and introduces resistive memory as a simpler alternative consisting of a single continuous strip of material between metal electrodes. It explains that resistance is controlled by 'set' or 'reset' voltages. A schematic illustration shows a resistive memory device with exposed cobalt oxide nanowires (blue) and gold electrodes (gold). The text concludes by stating that resistive memory relies on the formation and destruction of nanoscale, filamentary conductive pathways, and mentions the work of Takeshi Yanagida, Tomoji Kawai, and colleagues at Osaka University and Konkuk University in Korea.

Resistive memory: Total exposure

Resistive memory built with exposed, planar nanowires provides insights into resistive switching.

The current standard for non-volatile or 'flash' memory involves relatively complex structures. Much simpler is resistive memory, which consists of a single continuous strip of material between metal electrodes. The resistance across this material is forced low or high by applying 'set' or 'reset' voltages.

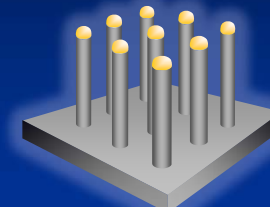
Resistive memory is known to rely on the formation and destruction of nanoscale, filamentary conductive pathways between the electrodes. However, the exact nature of these pathways is not completely understood, particularly for materials in which positive charge carriers are responsible for conduction, known as 'p-type' materials. Takeshi Yanagida, Tomoji Kawai and colleagues at Osaka University in Japan and Konkuk University in Korea have now revealed key details of resistive switching in p-type devices¹.

Schematic illustration of a resistive memory device consisting of exposed cobalt oxide nanowires (blue) and gold electrodes (gold)

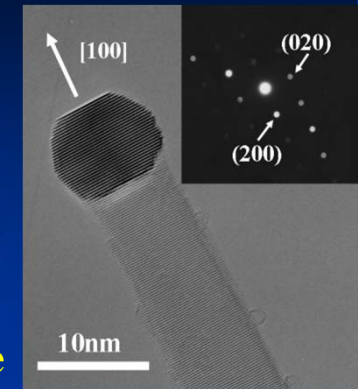
© 2011 ACS

Summary

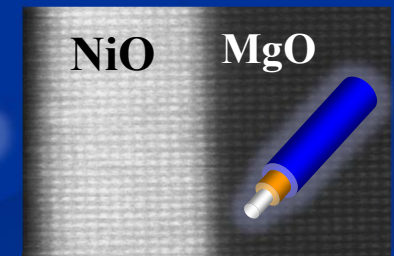
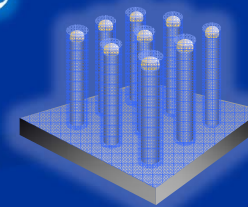
1. Fabrication of well-defined single crystalline oxide nanowires via VLS growth.



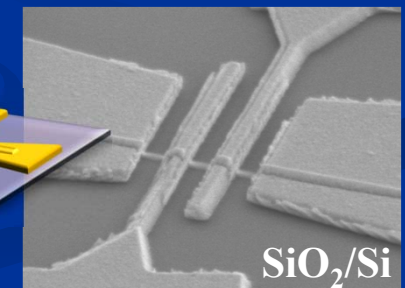
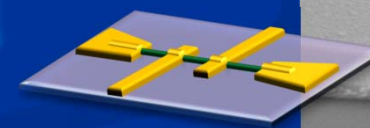
Single Crystalline
Oxide Nanowire



2. Creation of heterostructured oxide nanowires via novel in-situ technique.



3. Demonstration of nanoscale RS effects using oxide nanowire, and Extraction of RS nanoscale mechanisms for p-type oxides.



Single Oxide Nanowire Device!