Review on Device, Circuit and Antenna Technologies

for Terahertz Communication System

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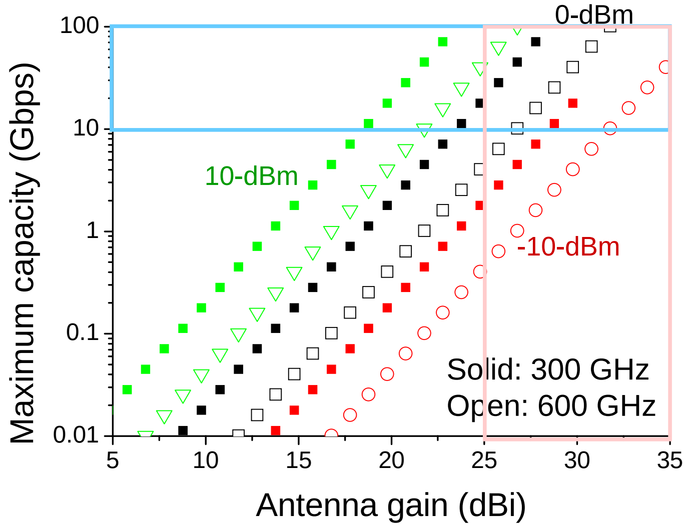
2010. 2. 2.

イントロダクション

テラヘルツ波のリンクバジェット

Frequency (GHz)	300 / 600
Loss in Air (dB/Km)	10 / 100
Distance (m)	5
Spectral efficiency (bit/Hz)	1 (ASK)
Radiated power (dBm)	0
Noise level (dBm/Hz)	-174
Noise figure (dB)	15
System margin (dB)	10



- 100 Gbpsまでの可能性を有する（以下の条件）

  Upto 100 Gbps is available. But at least,
  - approximately 1-mW output power
  - More than 25 dBi antenna gain

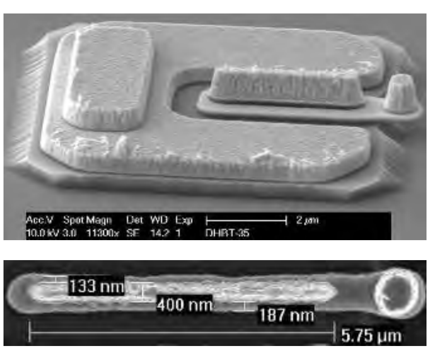
条件の詳細

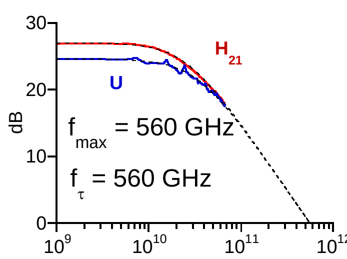
- 1-mW Output power in Tx
  - Tx output stage with 2-V / 5-mA DC, 10-% PAE
  - But, maybe poorer efficiency of around a couple of % in THz region.
  - Maybe come from huge loss even in ICs (conductive loss, dielectric loss)
- 15-dB Noise figure of Rx
  - Loss in front of LNA (eg. antenna feeding line) may cause problem in NF of Rx
- 25-dBi Antenna
  - Approximately, 1-cm long horn antenna provides 25-dBi gain
  - In case of arrayed antenna, more than 100 units of 5-dB patch are necessary
  - Beamsteering to overcome LOS operation
- Operating frequency
  - For 300-GHz amplifier, 400~600-GHz f_T/f_{MAX} devices are necessary.

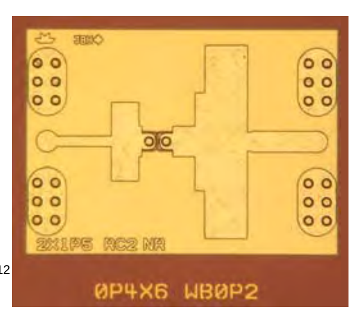
デバイス

III-V HBT

- R&D HBT, Rodwell Group, UCSB, USA
  - In 2008, HBT with 500-nm emitter-base junction width was commercialized by Teledyne (*f_T = 405 GHz*, *f_{MAX} = 392 GHz*)
  - 256-nm lab.-version device shows maximum f_T and f_{MAX} of 660 GHz and 780 GHz, respectively and ~3-V of BV_{CE}.
    - Applied to 300-GHz band amplifier (details later)
  - Aiming to 64-nm HBT with 1-THz f_T and 1.5-THz f_{MAX}

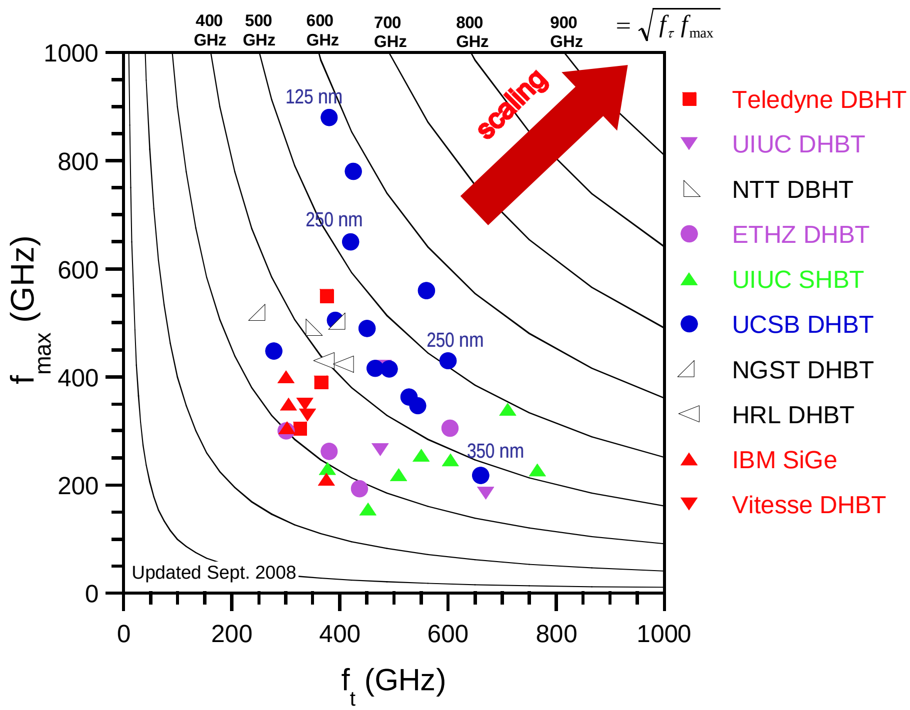






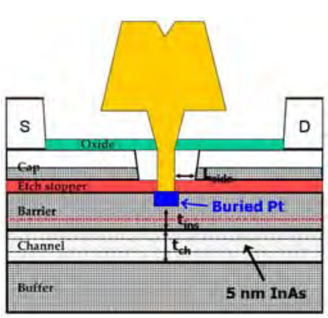
M. Rodwell, et al.,CSIC 2008

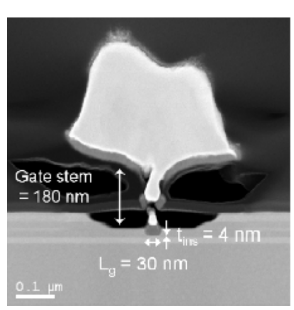
III-V R&D HBTsのトレンド (~2008)

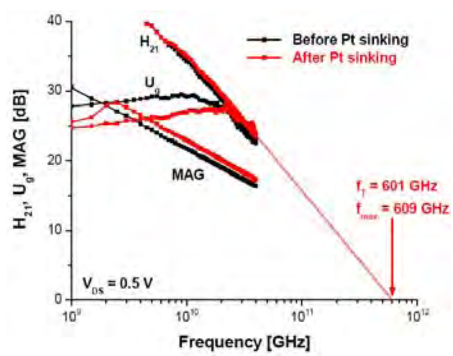


III-V HEMT

- R&D pHEMT, J. A. de Alamo Group, MIT, USA
  - Best record holder at 2009
  - 30-nm InAs/InP-HEMT: f_T / f_{MAX} = 601 / 609 GHz (IEDM2008)
  - 30-nm InAs/InP-HEMT: f_T / f_{MAX} = 628 / 331 GHz (EDL2008)
  - 50-nm InAs/InP-HEMT: f_T / f_{MAX} = 557 / 718 GHz (EDL2008)
  - But, main target of the development is for digital VLSI applications such as next generation microprocessor

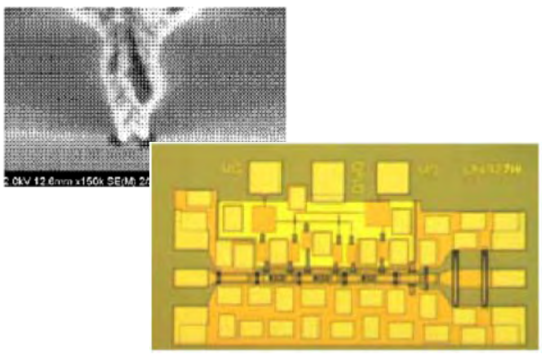


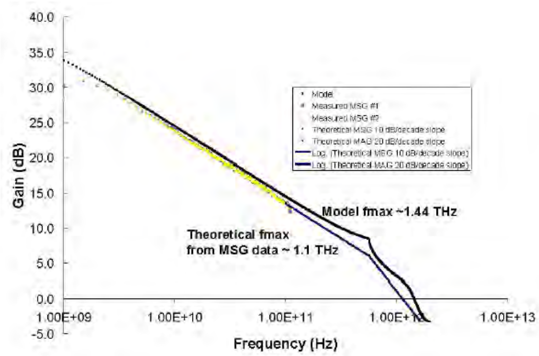




III-V HEMT

- R&D pHEMT, Northrop Grumman, USA
  - Former TRW, one of the major company for military and space system
  - Conducting 'Terahertz Electronics' program supported by DARPA
    - Started at April 2009
    - Development of transistor for MMICs operating at 670 GHz
  - InP HEMT with fmax greater than 1 THz (IEDM2007)
    - f_T = 385 GHz, f_{MAX} > 1 THz
    - Successfully applied to 300-GHz LNA





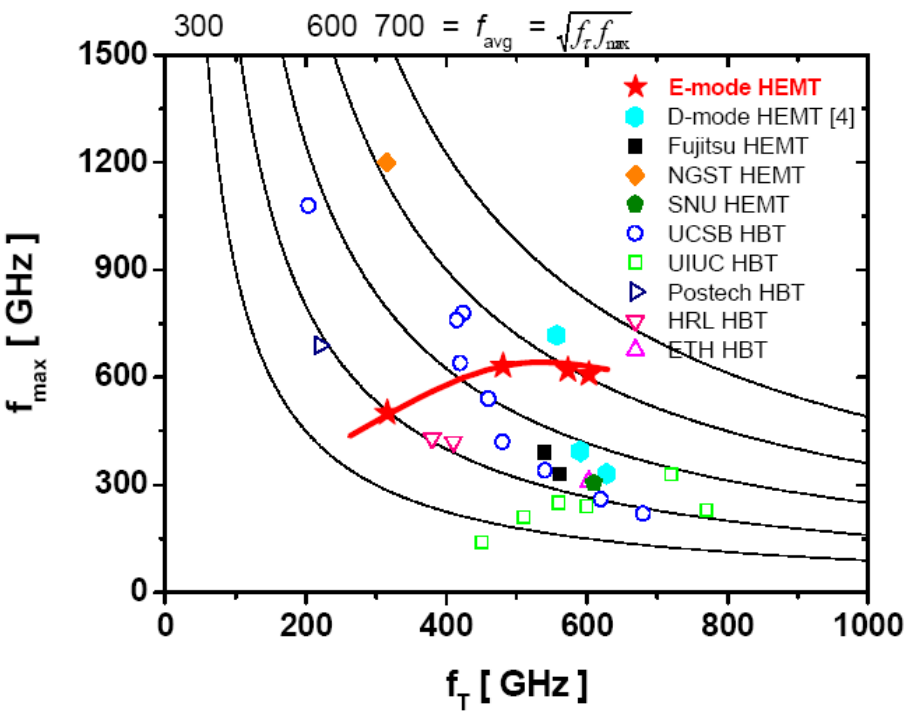
III-V HEMT

- Foundry service of III-V HFET
  - OMMIC, France
    - 70-nm MHEMT (f_T / f_{MAX}: 300 / 350-GHz)
  - Northrop Grumman, USA
    - 100nm InP HEMT (f_T / f_{MAX}: 180 / 350-GHz)
  - UMS (France)
    - 150-nm GaAs pHEMT (110-GHz cut-off)
    - Schottky diode (3-THz cut-off)

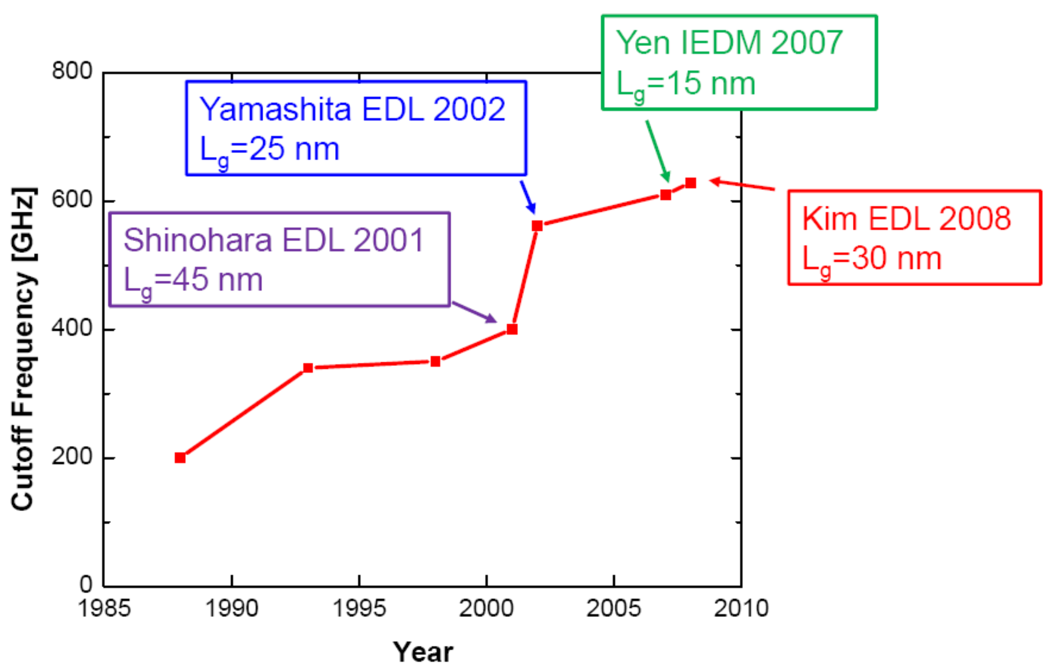
Process	ED02AH (PHEMT)	D01PH (PHEMT)	D01MH (MHEMT)	D007IH (MHEMT)	[illegible] (DHBT)
Gate length (µm)	0.18 or 0.15	0.13	0.13	0.07	1.5
Ft (GHz)	0.18 : 63 0.15 : 73	100	150	300	180
Fmax (GHz)	0.18 : 120 0.15 : 130	180	250	350	220
Vbgd (V)	8	12	10	3	BVce0 > 7
[illegible]	D : -0.9	[illegible]	D : -0.7	D : -0.5	-
[illegible]	[illegible]	[illegible]	Released	Preliminary	Preliminary

Parameter / Technology	1 um GaAs HBT	0.8 um Digital InP HBT	1 um Power InP HBT	0.15 um GaAs HEMT	0.10 um GaAs HEMT	0.10 um InP HEMT
Ft (peak)	40 GHz	140 GHz	80 GHz	80 GHz	120 GHz	180 GHz
Fmax (peak)	70 GHz	150 GHz	150 GHz	200 GHz	250 GHz	350 GHz
Beta / Gm	400	50	25	550 mS/mm	650 mS/mm	900 mS/mm
Breakdown	>13V BV CEO	>4V BV CEO	>13V BV CEO	13V BV gdr	7.5V BV gdr	2.5V BV gdr
Wafer Thickness	100 um	75 um	75 um	50 & 100 um	50 & 100 um	75 um
Airbridged Metal	Yes	Yes	Yes	Yes	Yes	Yes
[illegible]	[illegible]	[illegible]	s	Yes	Yes	Yes
[illegible]	[illegible]	[illegible]	ottky	Gate Source	Gate Source	Gate Source

R&D III-V HEMTのトレンド



R&D III-V HEMTのトレンド



- 寄生抵抗・容量の影響を除去することがゲート長を小さくすることより重要
  At this moment, eliminating parasitic effects is the key to improve device performance, not gate-length

Si-CMOS

- Large potential on cost, reliability and integration with other function blocks such as a DSP and RAM
- Limitation for THz-applications
  - high substrate loss → high signal loss and noise figure
  - low Gm → low gain
  - low breakdown voltage → low output power
- 65-nm bulk Si-CMOS was successfully applied to several ICs opearting in 100~200 GHz bands.
  - Expected f_T/f_{AMX} of 65-nm bulk Si-CMOS: 170/200 GHz

- R&D CMOS, IBM, USA (IEDM2007)
  - f_T of 485 GHz and 345 GHz for N-FET and P-FET in a 45-nm SOI CMOS process

Si-NMOS (CMOS)

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*35*	*32*	*28*	*25*
Performance RF/Analog [1]									
Supply voltage (V) [2]	1.2	1.1	1.1	1	1	1	1	0.95	0.85
T_{ox} (nm) [2]	2	1.9	1.6	1.5	1.4	1.3	1.2	1.1	1.2
Gate Length (nm) [2]	53	45	37	32	28	25	22	20	18
g_m/g_{ds} at $5 \cdot L_{min\text{-}digital}$ [3]	32	30	30	30	30	30	30	30	30
1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$) [4]	160	140	100	90	80	70	60	50	60
σV_{th} matching ($mV \cdot \mu m$) [5]	6	6	5	5	5	5	5	5	5
I_{ds} ($\mu A/\mu m$) [6]	13	11	9	8	7	6	6	5	4
Peak F_t (GHz) [7]	170	200	240	280	320	360	400	440	490
Peak F_{max} (GHz) [8]	200	240	290	340	390	440	510	560	630
NF_{min} (dB) [9]	0.25	0.22	0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2

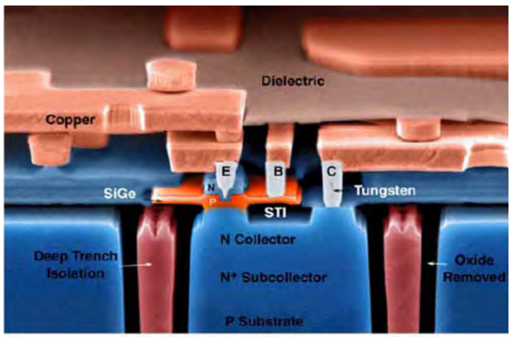
Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Performance RF/Analog [1]							
Supply voltage (V) [2]	0.8	0.8	0.8	0.8	0.75	0.75	0.7
T_{ox} (nm) [2]	1.1	1.1	1	1	0.9	0.9	0.8
Gate Length (nm) [2]	16	14	13	12	11	10	10
g_m/g_{ds} at $5 \cdot L_{min\text{-}digital}$ [3]	30	30	30	30	30	30	30
1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$) [4]	50	50	40	40	30	30	30
σV_{th} matching ($mV \cdot \mu m$) [5]	4	4	4	4	3	4	5
I_{ds} ($\mu A/\mu m$) [6]	4	3	3	3	2	2	2
Peak F_t (GHz) [7]	550	630	670	730	790	870	870
Peak F_{max} (GHz) [8]	710	820	880	960	1050	1160	1160
NF_{min} (dB) [9]	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2

http://www.itrs.net/

SiGe HBT

- Lower cost than III-V device, compatible with Si-CMOS
- Comparing to CMOS, SiGe HBT has several merits such as higher Gm, larger Zout, easier matching and smaller 1/f noise.
- But, extra cost is required for SiGe processes on baseline CMOS fab.

- TMTT2004, SiGe HBT, IBM, USA
  - Up to 9HP processes (0.13-*u*m, f_T / f_{MAX} = 350 / 300-GHz) are developed
  - IBM serves the 8HP (0.13-*u*m, f_T / f_{MAX} = 210 / 285-GHz) process as a foundry service.
  - Successfully applied to 100-GHz bands ICs. (details later)

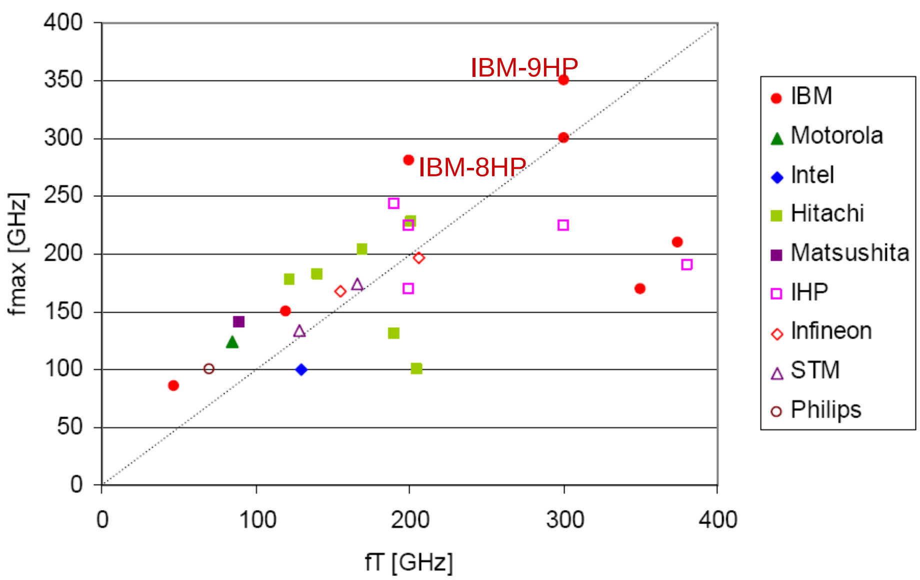


	5HP 6HP	7HP	8HP	9HP
f_T [GHz]	47	120	210	350
f_{max} [GHz]	85	150	285	300
$J_{c,p}$[mA/μm²]	~1.5	~8	~12	~19
BV_{CEO} [V]	3.4	1.8	1.7	1.7
BV_{CBO} [V]	10.5	6.5	5.5	5.6
Beta	100	300	300	650

SiGe HBTのトレンド

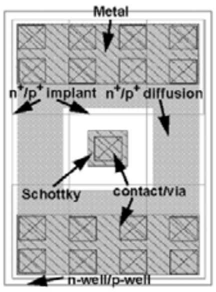
- 速度増加は面積と厚さを小さくすることで達成され、走行時間や寄生抵抗・容量の減少をもたらした.

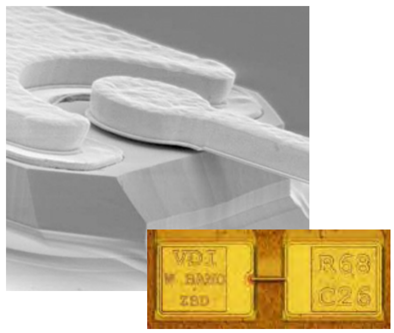
The speed enhancement was primarily achieved through vertical and lateral scaling, resulting in the reduction of transit time and parasitic resistance and capacitance.

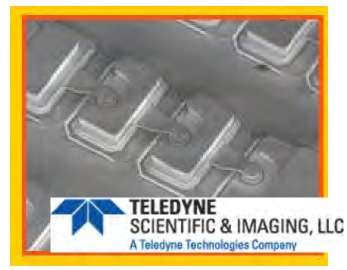


Schottky Barrier Diode

- SBDs working over 1 THz are available with almost all materials
  - CMOS
    - Florida Univ. reports CoSi2-Si SBD working over 1.7 THz with bulk-Si 130-nm CMOS proecss
    - Resistance and capacitance of > 10 Ω and 8 fF, respectively
  - GaAs
    - Virginia Diode Inc.: > 3 THz, discrete and full-customized foundry
    - Teledyne SI.: > 2 THz, discrete
    - UMS: >3-THz, full-customized foundry







UTC-PDs

- High speed and high output power by uni-carrier operation
- Speed performance mainly relies on the junction size of the device
- NTT, Japan
  - 500 uW@350 GHz, 11 uW@1.1 THz (Fig. 1~3) with resonant type devices (IRMMW-TH2008)
  - 2.3 uW @ 1.0 THz (Fig. 4) with wideband type devices integrated with a log-periodic antenna (JLT2005)

Fig. 1

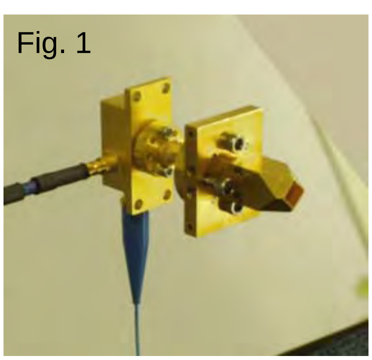


Fig. 2

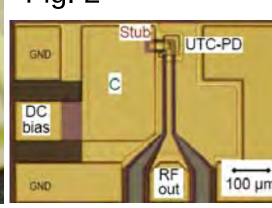


Fig. 3

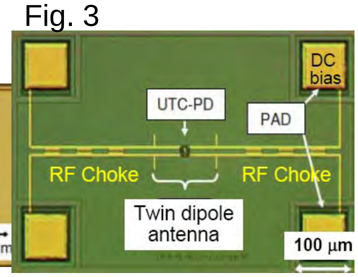
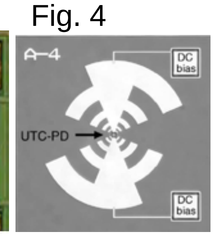
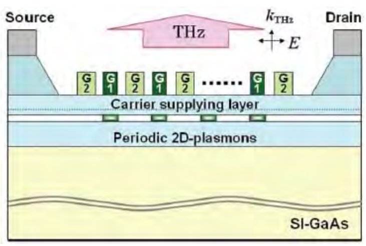


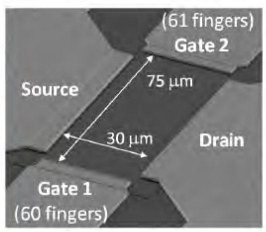
Fig. 4

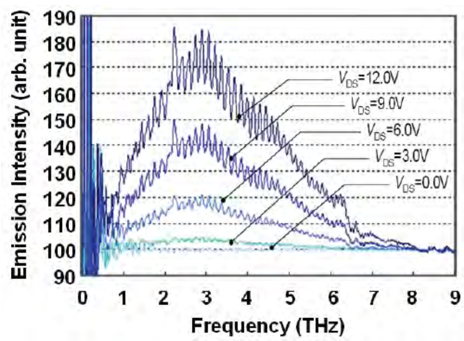


Plasmonic Devices

- Plasmon resonance of two-dimensional electron system which would exist in HEMT structure
  – Resonance frequency is function of a gate length in HEMT structure
  – Sub-micro HEMT can be utilized as a emitter or detector of THz waves
- Otsuji Group, Tohoku Univ. Japan
  – InGaP/InGaAs/GaAs HEMT structure with interdigitated dual-gates
  – THz radiation in 0.5~3 THz with ~uW power



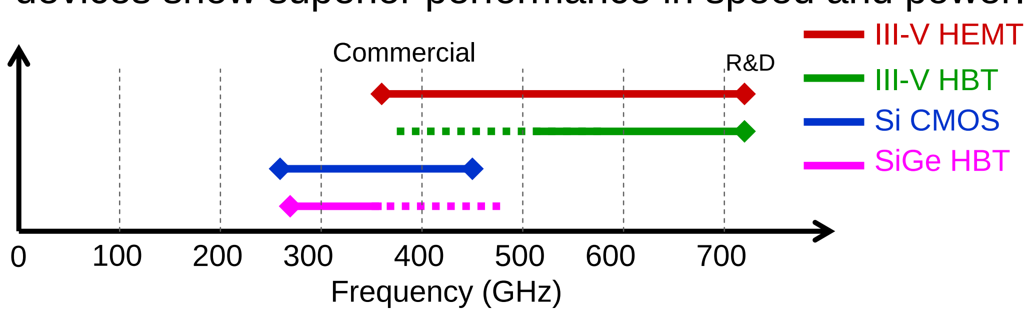


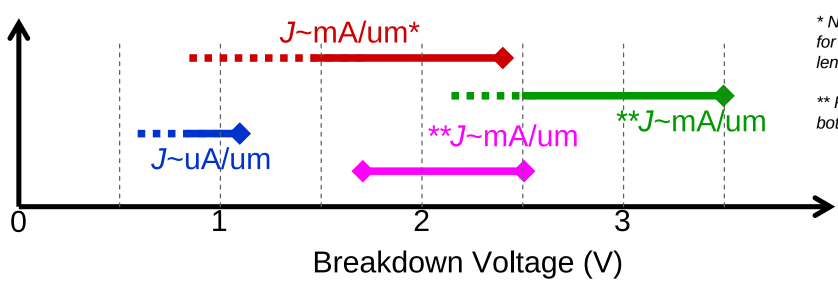


デバイスの現状

- III-V デバイスはスピードと出力に関する優れた性能を示す.

  III-V devices show superior performance in speed and power.

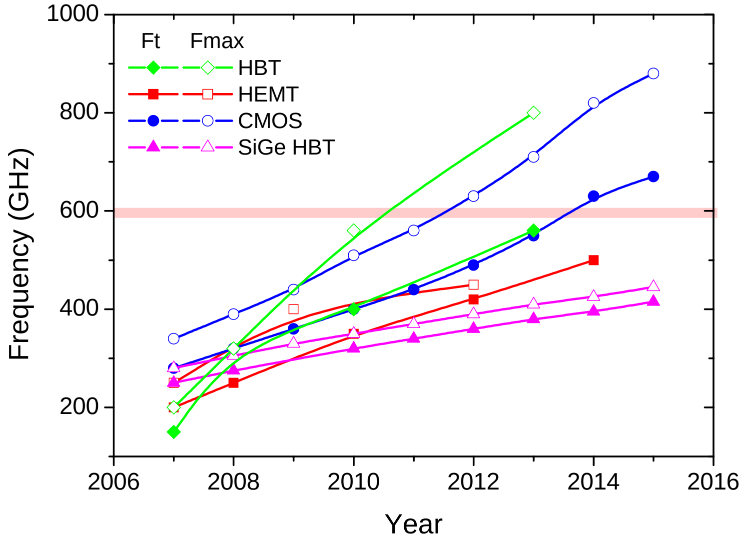




** Normalized by gate length for FETs or EB- junction lengths of HBT*

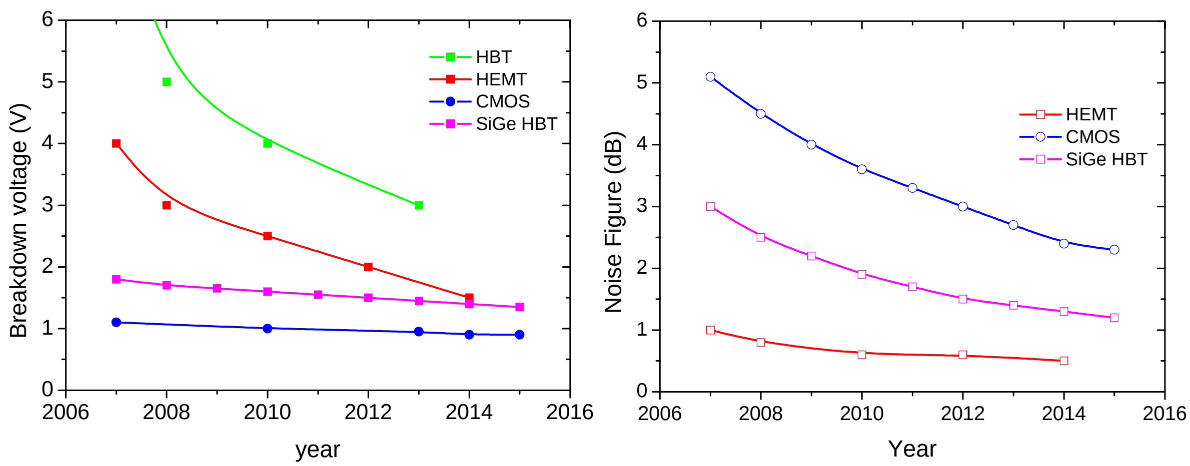
*** For 0.13-um width for both III-V and SiGe HBTs*

ITRS2007: 市場からの要求



- Commercial CMOS will reach to 600-GHz in a few years based on advanced fabrication technology (lithography, chemical, etc..).
- For HBT, margin on scaling (256-nm → 64-nm)
- For HEMT, gate length reach to near physical limitation.
  - But 1-THz device would be available by reducing parasitic effect. (TWHM2009, del Alamo, MIT,)

ITRS2007: ミリ波から要求



- But, CMOS may offer limited performance in output power and noise
  - On the other hand, III-V devices have still merits in performance

まとめ: デバイス

- 研究用途としては 700-GHz HEMT/HBTs, 480-GHz Si-MOSs が報告されている.

  For R&D device, 700-GHz HEMT/HBTs and 480-GHz Si-MOSs are available at this time.
  - Scaling was main issue. But further improvement will be on how to suppress parasitic component for all of devices.
- 商用のファウンドリサービスとしては, 200~300 GHz の III-V and Si デバイスでの可能性がある.

  For commercial foundry services, 200~300 GHz devices are available with both of III-V and Si devices.
  - According to ITRS roadmap (*RF/AMS Technologies* section), progress of Si-devices would be much faster than III-V devices, probably due to market issue.
- ショットキーはTHz周波数応答を持つ.

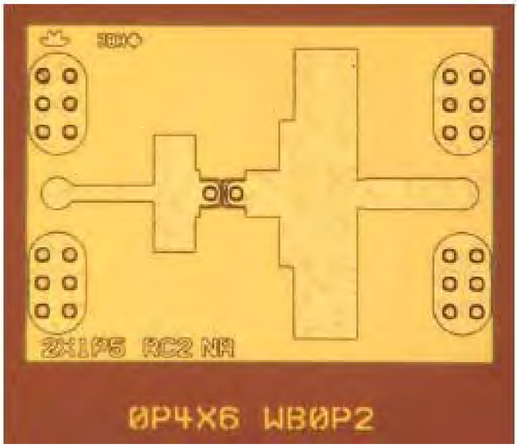
  Schottky diode for THz operation is available.

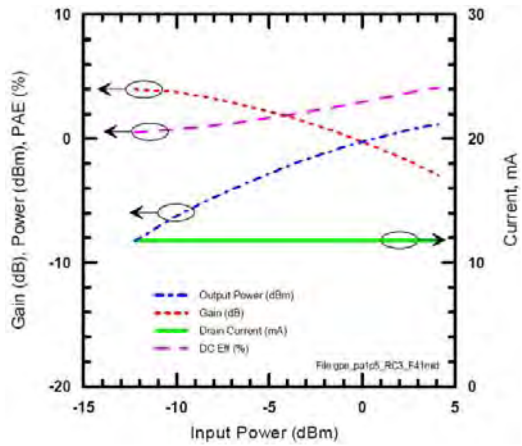
回路

HBT/HEMT/CMOS/SiGeHBTの利用

HBT: 324-GHz Amplifier

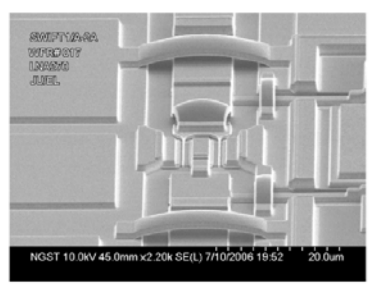
- IMS2008, Teledyne+UCSB, USA
  - 250-nm InP HBT (f_T/f_{max}=>373/550 GHz)
  - Single stage amplifier
    - 4.8-dB Gain @ 324 GHz
    - ~1.3-mW Psat @ 324 GHz (PAE of < 2-%)
    - Microstrip line transmission line (h_{BCB}=10 um)

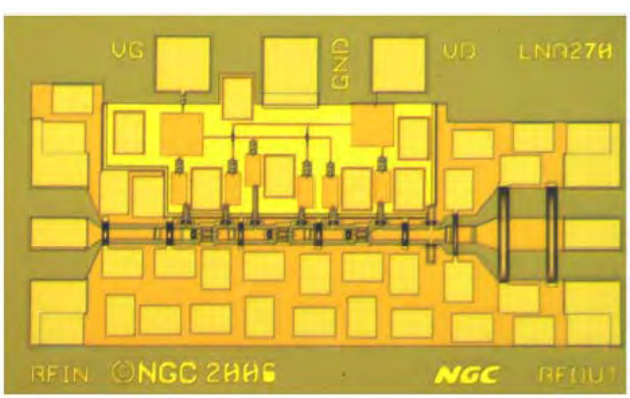


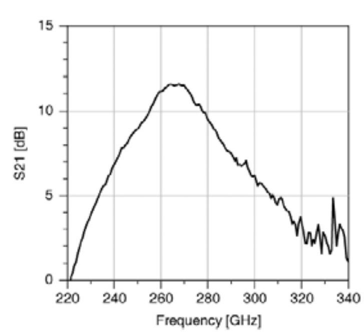


HEMT: 270-GHz Amp.

- MWCL2007, Northrop Grumman, USA
  - 3-stage amplifier with 35-nm InP pHEMT
  - 11.6-dB Gain @ 270-GHz
  - 7.5-dB NF @ 270-GHz
  - DC power: 0.8-V / 13.8 mA (~11 mW_{DC})
  - GCPW transmission line (h_{CPW}=620um)

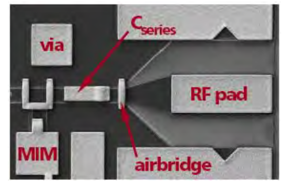


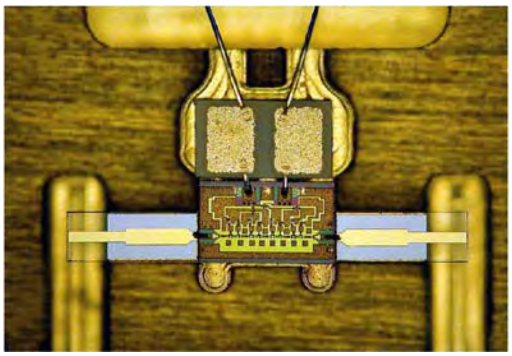


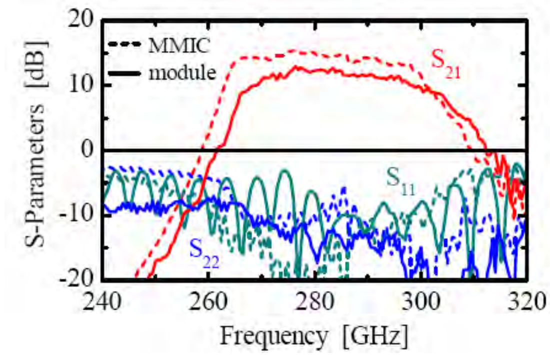


HEMT: 300-GHz Amplifier module

- IPRM2009, Fraunhofer Institute (IAF), Germany
  - 35-nm InAlAs/InGaAs mHEMT (f_T/f_{max}=515/700 GHz)
  - GCPW transmission line with VIA process (g_{CPW}=14 um, h_{SUB}=50 um)
  - Single stage amplifier.
    - > 5-dB gain in 258~308 GHz
  - 4-stage amplifier
    - 12~13-dB gain in 264~300 GHz
  - H-band wagveguide transition with probe-type transition on quartz



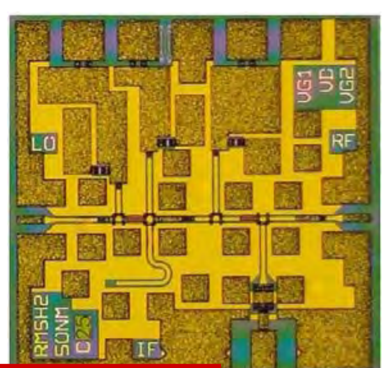




HEMT: 300-GHz Freq. doubler + Mixer

- EuMIC2009, Fraunhofer Institute (IAF), Germany
  - 50-nm InAlAs/InGaAs mHEMT (f_T/f_{max}=400/420 GHz)
  - Frequency doubler
    - > 10% conversion efficiency
    - -6.4-dBm Psat @ 310 GHz
    - -9.5-dBm Pavg in 250~310 GHz
  - Doubler + Mixer
    - 20-dB conversion loss in 246~300 GHz
    - Resistive mixer

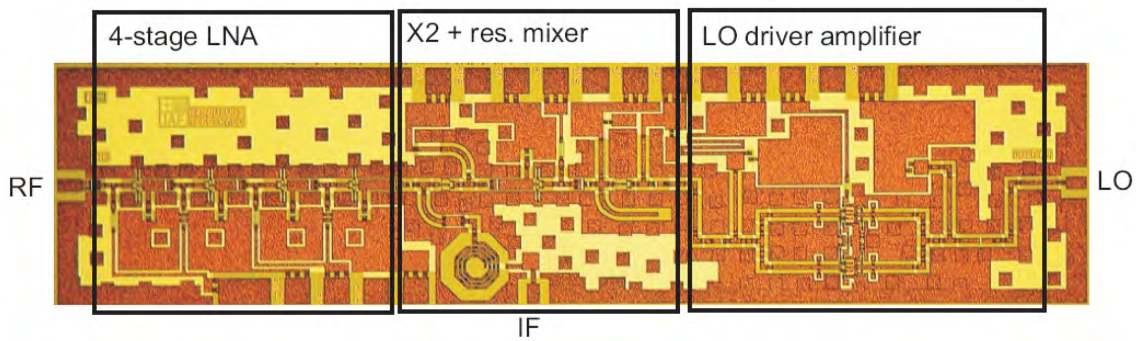
Doubler



Doubler+mixer

HEMT: 200-GHz Active Receiver

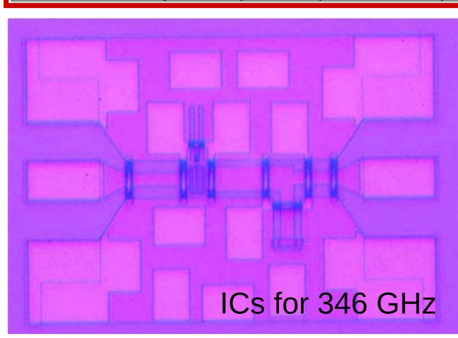
- EuMIC2009, Fraunhofer Institute (IAf), Germany
  - 100-nm InAlAs/InGaAs mHEMT (f_T/f_{max}= 220/300 GHz)
  - LNA + HEMT Mixer + LO-freq. doubler + LO driving amplifier
  - 7-dB Conversion gain @ 200-GHz, -13 dBm LO driving
  - Chip: 1x4 mm^2

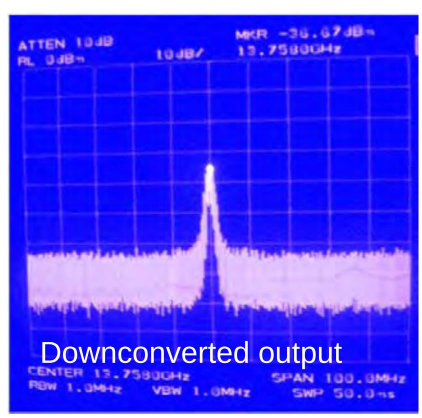


HEMT: 346-GHz Oscillator

- MWCL2007, Northrop Grumman, USA
  - 35-nm InGaAs/InP HEMT (f_T/f_{max}= ?? / 600GHz)
  - Common gate for conditional stable
  - GCPW transmission line (h_{CPW}~630 um)

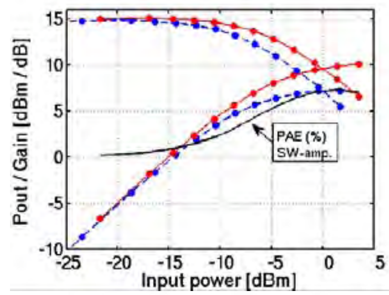
Frequency of Oscillation (GHz)	Vds (V)	Ids (mA)	Measured Output Power (μW)	DC to RF Efficiency (%)
254	1.3	9	158	1.35
314	1.2	6	46	0.64
346	1.3	9	25	0.21

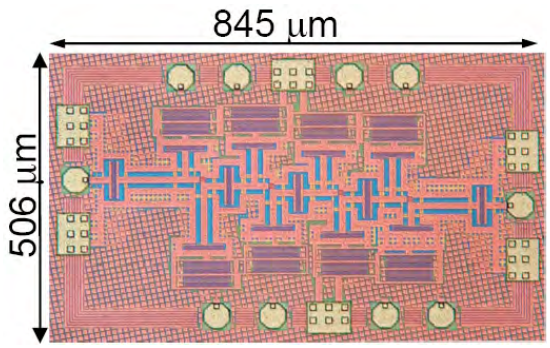


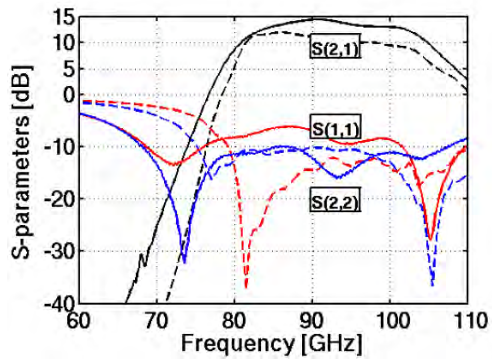


CMOS: W-band Amp.

- ISSCC2009, Sandstorm, et al., TKK-HUT, Finland
  - 65-nm Si-MOS
  - 4-stage common source
  - 80 ~ 100 GHz
  - G_{peak} = 13 dB, P_{sat} = 10.0 dBm (PAE=7.3%)
  - NF = 8.5~7.5 dB



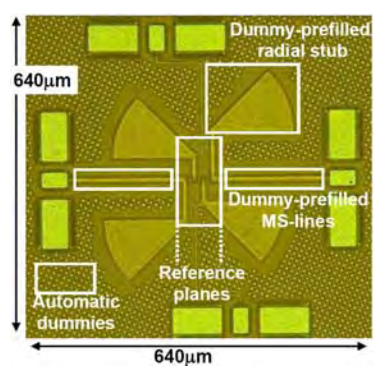


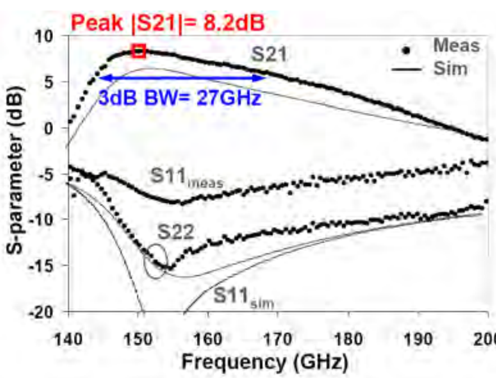


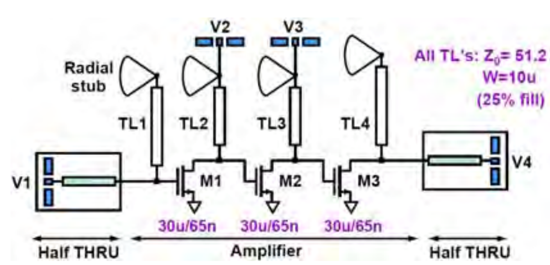
CMOS: 150 GHz Amp.

- ISSCC2009, M. Rodwell group, UCSB, USA
  - 65-nm digital Si-CMOS
  - 3-stage common source
  - 150 GHz (f_{-3dB}=27 GHz)
  - G_{peak} = 8.2 dB, P_{sat} = 6.3 dBm

    (Pads were deembedded)

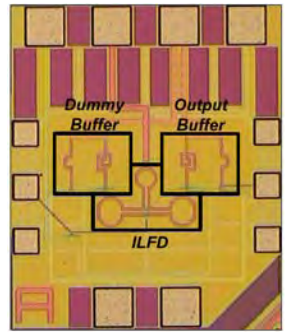


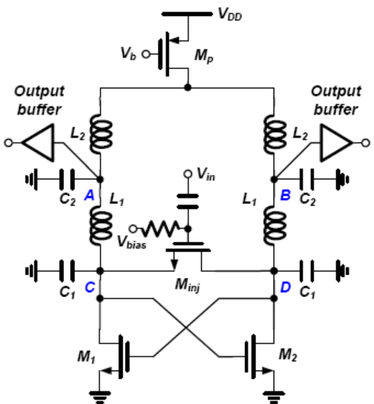


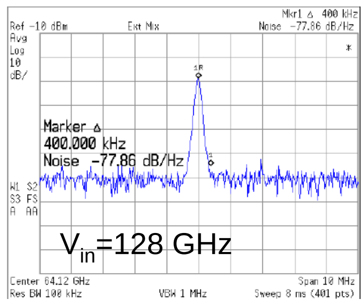


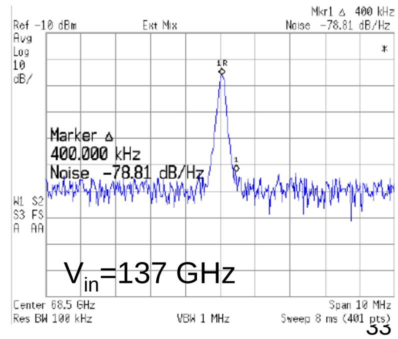
CMOS: 128-137GHz frequency divider

- ISSCC2009, Liu Group, National Taiwan U., Taiwan
  - 65-nm Si-MOS
  - Injection Locking type
  - 128~137 GHz locking range
  - Output power < -24 dBm
    - <1-% conversion efficiency



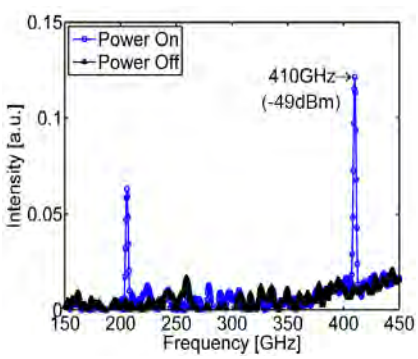


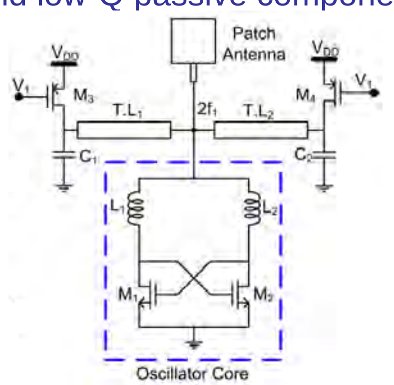


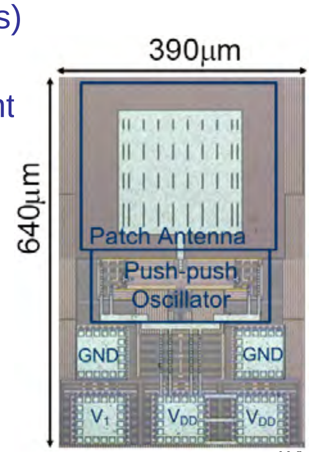


CMOS: 410-GHz oscillator

- ISSCC2008, K.K.O Group, Florida U., USA
  - 45-nm low-leakage Si-MOS
  - Push-Push 2nd harmonic oscillator
  - Integrated patch antenna
  - -49-dBm @ 410 GHz
    - No gain from 200-GHz output buffer
    - Very low efficiency of antenna (< 20%, 7dB loss)
    - Antenna mismatching loss (~2dB)
    - Loss in substrate and low-Q passive component

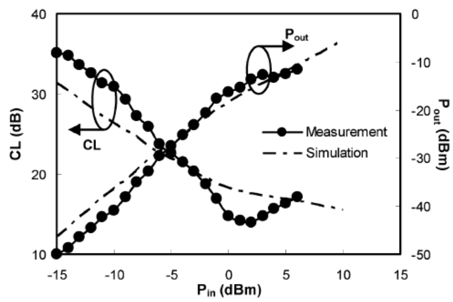


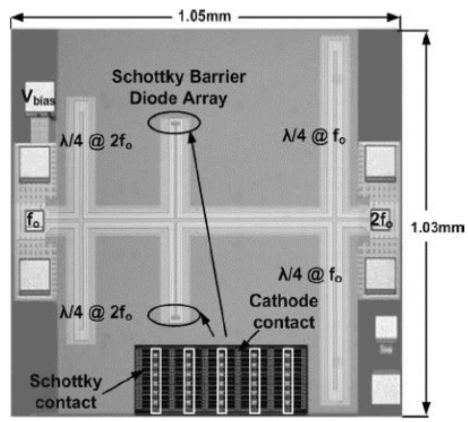




CMOS: SBD frequency doubler

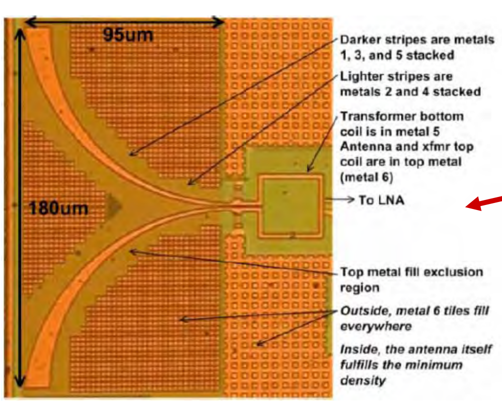
- MWCL2009, K.K.O Group, Florida U., USA
  - 130-nm UMC CMOS process
  - SBD: 3-um^2 effective area,
    - 14-Ω R_S, 15-fF C_J → ~750-GHz cutoff
    - 500-uA bias current
  - 128~134 GHz 3-dB BW
  - 14-dB conversion loss @ 134 GHz
    - -11 dBm output power
    - 14-dB fund. rejection @ output

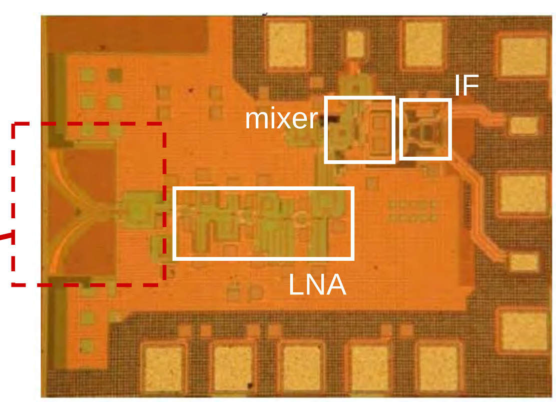




CMOS: 140-GHz receiver

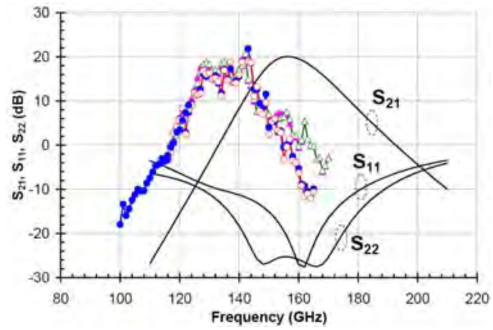
- RFICS2008, Nicolson et al., U. of Toronto, Canada
  - 65-nm STMicroelectronics GP CMOS (f_T/f_{max}=170/240 GHz)
  - Tapered antenna + LNA + downconverter + IF amp.
    - Total CL: 15-19 dB in 100-140 GHz
    - Antenna loss ~ 25 dB **!!**
    - LNA: 8-dB gain, -1.8-dBm P_{sat}
    - Mixer: 5-dB CL, 22-dB NF

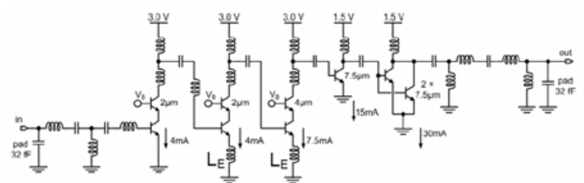


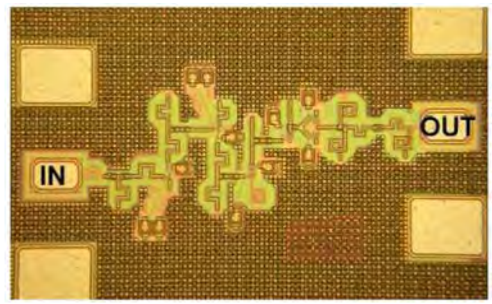


SiGe HBT: 140-GHz Amp.

- RFICS2007, Laskin et al., U. of Toronto, Canada
  - STMicroelectronics SiGe HBT (f_T/f_{max}=230/300 GHz)
  - 5-stage cascode
  - 17-dB gain @140 GHz, 1-dBm Psat

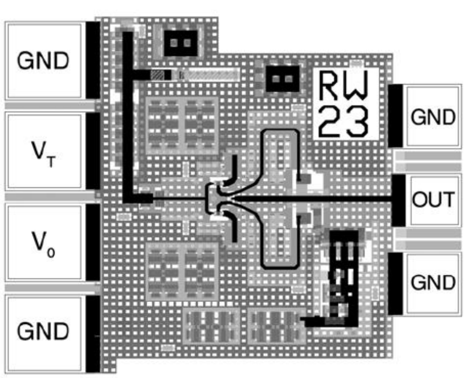


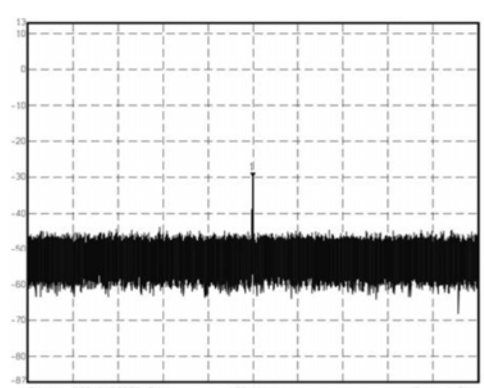




SiGe: 278-GHz Push-Push VCO

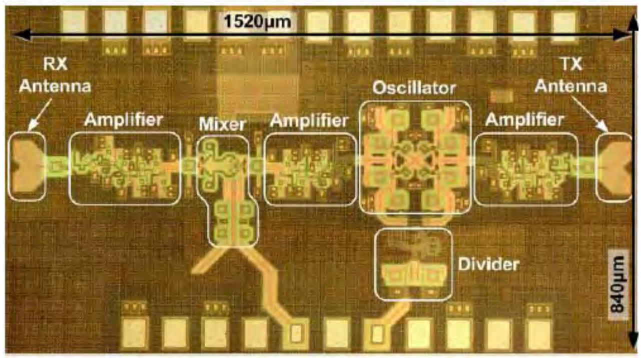
- IMS2007, Wanner et al., Technische Univ., Germany
  - Infineon SiGe HBT (f_T/f_{max}=270/340 GHz)
  - Push-Push configuration.
    - -20~-25-dBm output power in 275.5~279.6 GHz





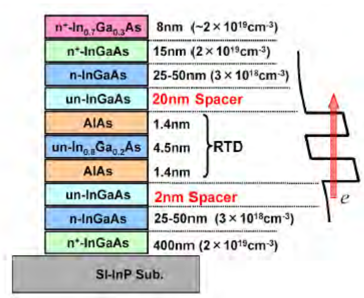
SiGe: 170-GHz Transceiver

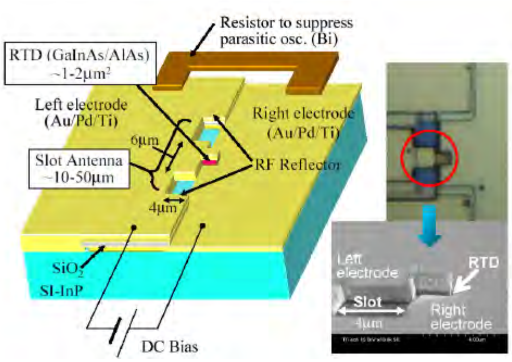
- RFICS2008, Laskin et al., U. of Toronto, Canada
  - SiGe HBT (f_T/f_{max}=270/340 GHz)
  - Tx/Rx-antenna, Tx/Rx amplifier, Rx mixer, 165-GHz Osc.
    - Amplifier: 15-dB gain, 0-dBm Psat in 166~174 GHz
    - Receiver: ~21-dB noise figure w/o antenna
    - Transmitter: -5-dBm output power w/o antenna
    - Antenna: dipole antenna, 21-dB loss

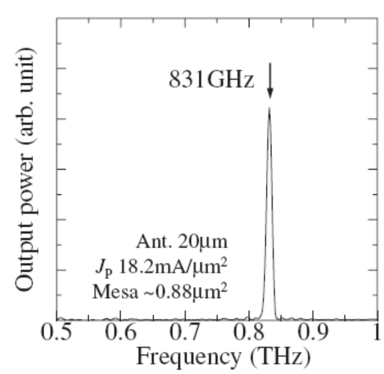


RTD Oscillator

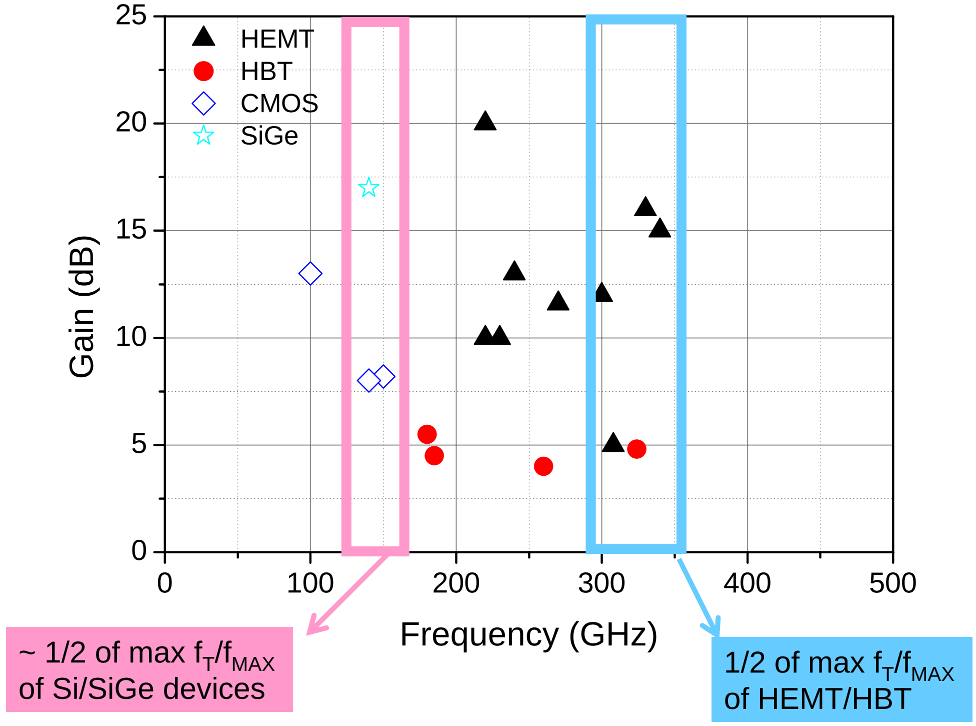
- TeraTech2009, Asada Group, TIT, Japan
  - Fundamental Oscialltion
    - -8-dBm @ 270-GHz
    - -7-dBm @ 470-GHz
    - -30-dBm @ 831-GHz
  - Harmonic Osciallation over 1 THz



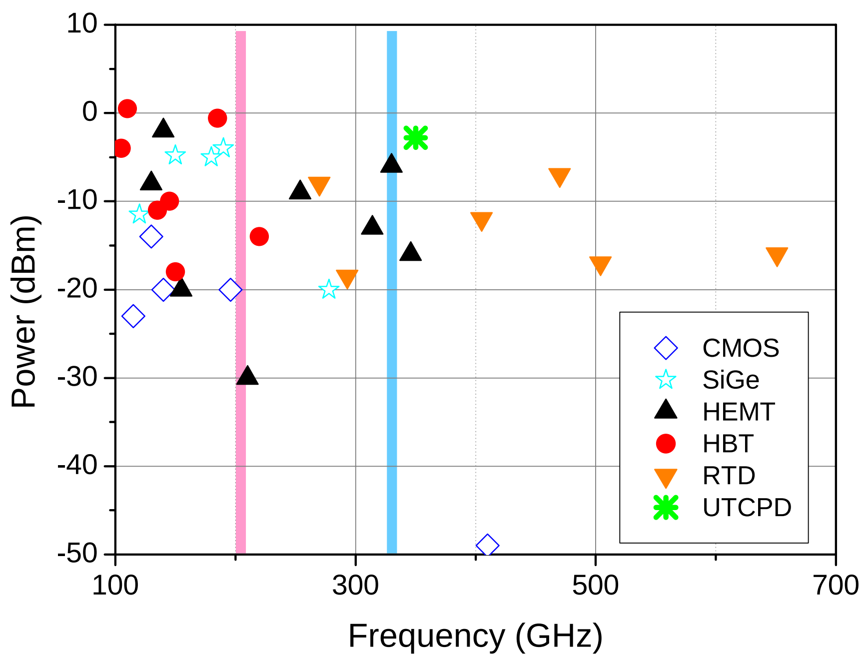




アンプのトレンド



オシレータのトレンド



まとめ: 回路

- III-V HBT
  - Amplifiers upto 300 GHz
  - No recent activity in MMICs
- III-V HEMT
  - 300~400 GHz circuits with 50~30-nm HEMTs (f_T of ~500 GHz)
  - Amp., mixer, freq multiplier, oscillator are available
- Si-CMOS
  - Upto 150-GHz operation is available with 90~65-nm CMOS process (f_T of ~270 GHz)
  - Amp., mixer, freq multiplier, oscillator are available
- SiGe HBT
  - Not so many reports (maybe due to less foundry company?)
  - Upto 200-GHz operation would be OK with 130-nm process

回路の今後

- CMOS を使った300-GHz MMICは数年以内に実現
  300-GHz MMICs with CMOS in a few year
  - MMICs works upto around half of cut-off frequencies of transistors
  - Cut-off frequency of Si-CMOS will exceed 600-GHz in a few years
- 利得と出力向上のための効率化
  Better efficiency for better gain and output power
  - Very poor efficiency of 1 % or less was presented in current works
  - 1 %→ 10 % efficiency improvement cause 10-dB improvement
  - Reducing dielectric and conductive losses in ICs.

アンテナ

On/Off-Chip Antennaの特徴

- On-chip antenna
  - ☺ No interconnection loss between chip and antenna
  - ☺ Expectable matching performance between chip and antenna based on 3D-EM simulation and stable fabrication
  - ☹ Difficult to enhance radiation efficiency due to fixed substrate. Eg. Si-CMOS
  - ☹ Higher modes in high-dielectric constant substrate (Si, InP, GaAs)
  - ☹ Limited chip area ? (but, no-big problem in THz region)

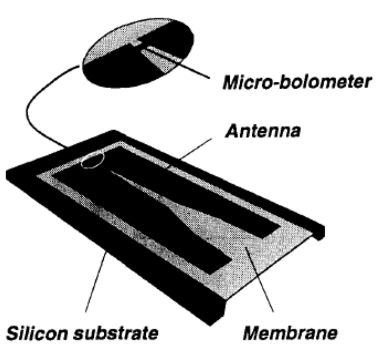
- Off-chip antenna
  - ☺ Possible to select optimum material for antenna
  - ☺ External cavity (but, too small to fabricate at 300 GHz. $\lambda_{air}/4$~250 um)
  - ☹ Interconnection/transition loss should be minimized between chip and antenna
  - ☹ Maybe bulky due to waveguide-based structure

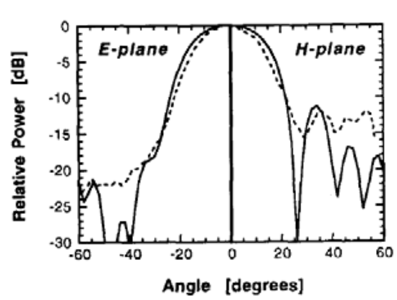
プリントアンテナの特徴

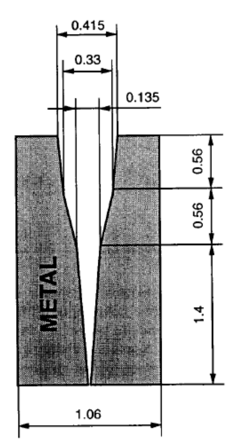
- Radiation efficiency
  - Dielectric loss of substrate suffer the efficiency directly
  - Dielectric constant of substrate ⇑ → higher substrate mode ⇑ → efficiency ⇓
- Gain
  - Extra cavity or reflector enhance the bandwidth and gain
  - Arrayed antenna
    - Improving antenna directivity
    - Additional gain *vs*. Additional loss from feeding network
- Feeding line
  - Multi-level substrate is difficult to implement in THz region due to large inductance of VIA structure
  - Need to suppress higher modes in feeding line

On Chip: Tapered Slot Antenna

- TMTT1993, Chalmers Univ. & NASA, USA
  - Tapered slot antenna on dielectric membrane for 802 GHz
    - 1.7-um SiO2/Si3N4 dielectric film
    - Dry-etching of Si-substrate
  - 13-dB and 50-% of directivity and radiation efficiency
  - -10-dB beamwidth ~ 40^{o}
  - Longer antenna shows narrower beam ~ 4^{o} of 3-dB beamwidth

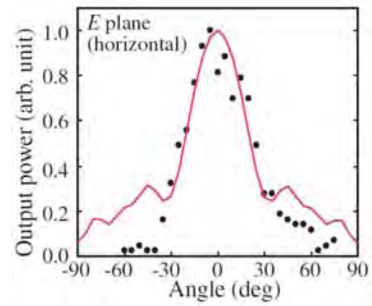


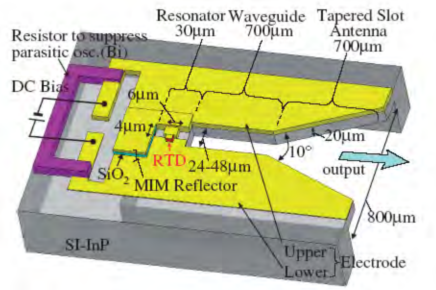


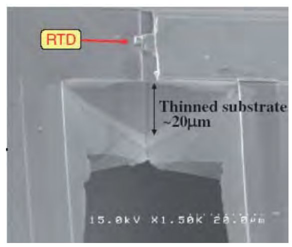


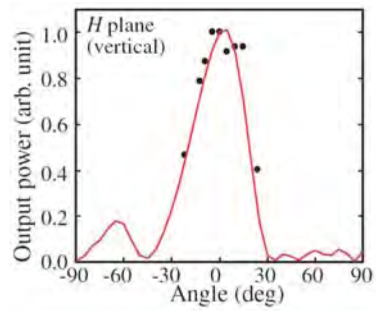
On Chip: Tapered Slot Antenna

- APEX2009, Asada Group, TIT, Japan
  - 405-GHz fundamental oscillator
    - 60-uW output power
  - Full removal of substrate using wet etching
    - 20-um thick substrate under antenna
    - Air in slot
  - 45º and 40º in E/H plane, respectively
    - 8.6-dBi directivity from 3D EM simulation



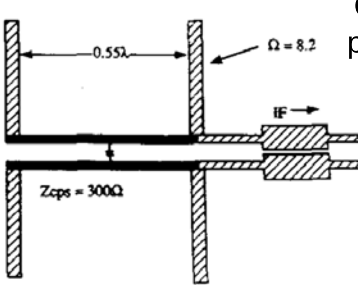


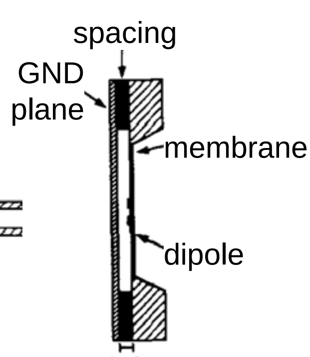


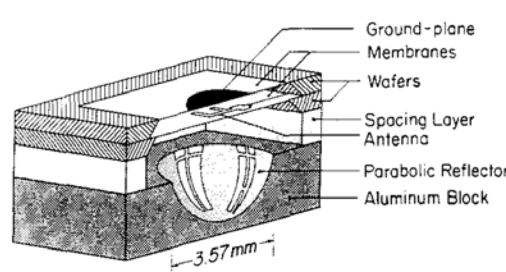


On Chip: Dipole Antenna with Reflector

- TMTT1992, NASA, USA
  - Double-dipole antenna for 246 GHz
    - on 1-um dielectric membrane (4 x 4 mm^2)
    - Back ground reflector
    - 12~13-dBi gain at 246-GHz
  - External parabolic reflector
    - 119-um diameter reflector
    - Total measured gain ~ 37 dBi

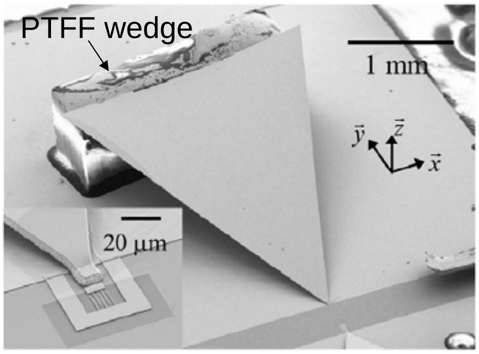


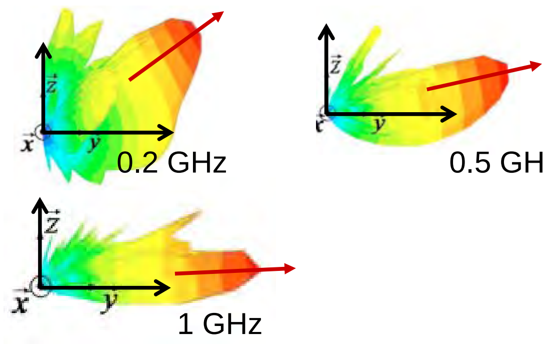




On Chip: TEM Horn antenna

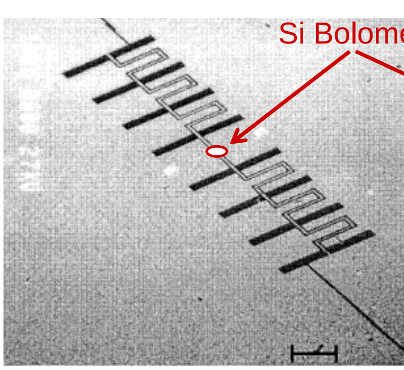
- APL2008, CNRS, France
  - Fabrications
    - Bottom ground → interlayer deposition → top triangle metal for horn → etching interlayer → Drying with CO2 drier → lifting up top metal with micromanipulator → placing PTFF wedge and fixing
  - Broadband operation over 1 THz
  - EM-beam direction changes with frequencies, probably due to the PTFF wedge on the beam path



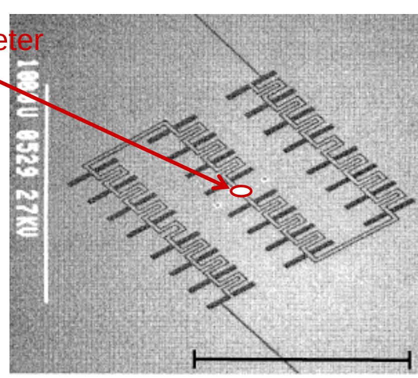


On Chip: Slot-Array Antenna

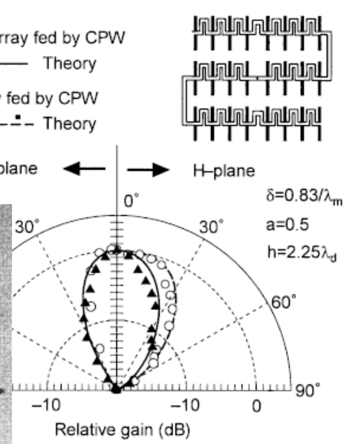
- IEICE1999, Kobayashi et al., NDA, Japan
  - 700-GHz Slot array antenna with CPW feeding
    - On Fused quartz (h_{quartz} = 500 um)
    - 8-slot antenna: 11-dBi gain
    - 8x3 slot antenna: 13-dBi gain



100 μm

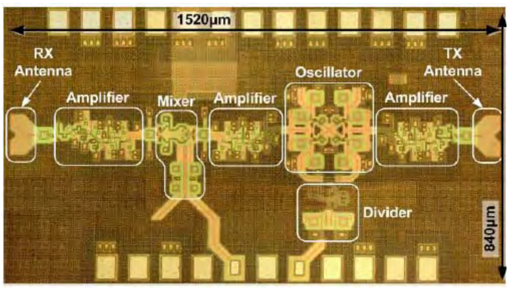


1000 μm

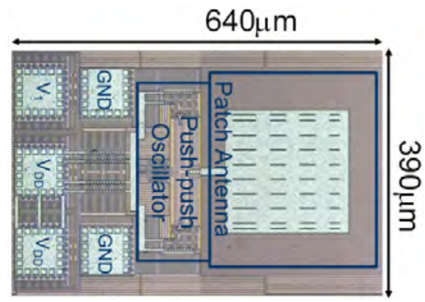


On Chip: Antennas on Si-ICs

- RFICS2008, Laskin et al.,
  - Dipole (tapered slot ??) antenna with SiGe process
  - 21-dB loss from antenna
- ISSCC2008, K.K.O Group
  - Patch antenna for 410-GHz
  - 20% radiation efficiency + material loss + mismatching, etc…



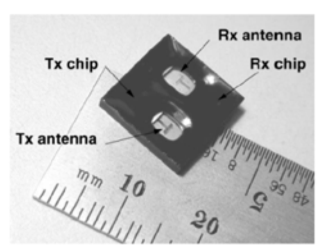
RFICS2008, Laskin et al.,

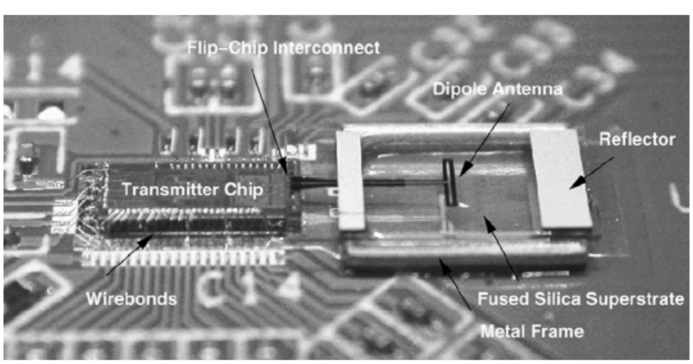


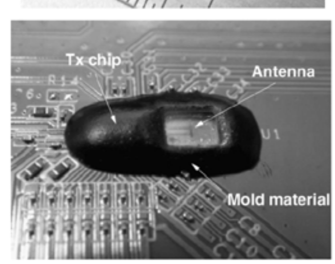
ISSCC2008, K.K.O Group

Off Chip: Cavity-Backed Slot Antenna

- TMTT2006, IBM, USA
  - Chip scale packaging for 60-GHz radio
  - Slot antenna on Quartz with optimized backed-cavity
    - Kovar alloy for cavity-wall, which works as a antenna support
    - Over 90% radiation efficiency
    - 8-dBi antenna gain, ~10% gain-bandwidth
    - Suppressed surface modes with cavity
  - Flip-chip bonding

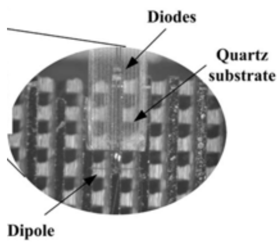


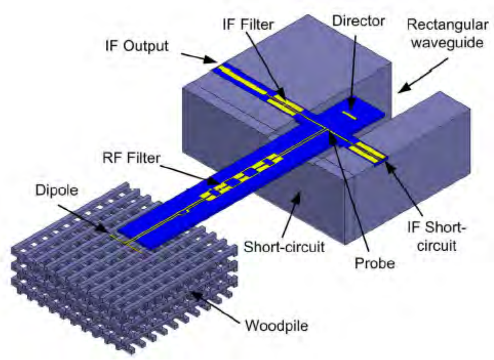


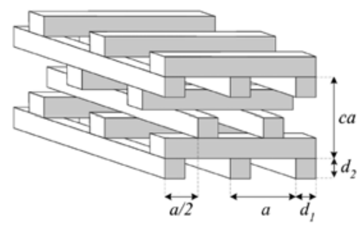


Off Chip: Metamaterials

- TAP2007, Universidad Pública de Navarra, Spain
  - Dipole antenna on metamaterial
    - Dipole on Quartz + Si-metamaterials
    - Work as a back-reflector → high directivity
    - Suppress parasitic surface waves
    - a=0.36 mm, ca=0.62 mm, d1=d2=0.155 mm
    - Silicon woodpile: 5 periods in vertical, 15-periods on lateral plan



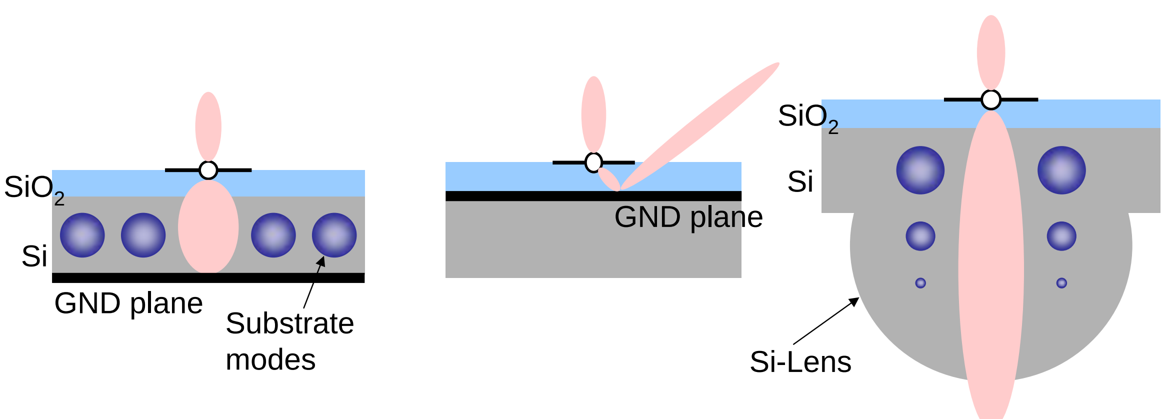




Hemisphere Silicon Lens

☺ Suppress the amount of unwanted substrate modes

☺ Collimating EM-wave → enhancing directivity of antenna



☹ Spatial aliment is critical in performance

☹ Difficulty in bonding process

☹ No broadband AR coating for Si-lens

まとめ: アンテナ

- オンチップアンテナの利得は10~14-dB 程度
  Around 10~14-dB antenna gain from on-chip antennas
  - Using micromachining, arrayed configuration
  - Radiation efficiency is issue as well, especially on silicon substrate
- オフチップ（平面型）の利得は10-dB程度
  off-chip antenna offers around 10-dB gain, too
  - But, better efficiency and wider bandwidth due to optimized substrate and structure
- 300-GHz 通信に必要な25-dBには現状では及ばない
  Far away from 25-dB gain for 300-GHz communication
  - Extra lens or cavity to improve gain
  - Share of gain load with Tx (output power) and Rx (noise figure)

まとめ

- III-V デバイスは 300-GHz ICを提供可能
  Current state of art III-V devices provide 300-GHz ICs
  - 1-THz III-V devices is technically feasible.
  - But, difficult to access these technology due to few provider
- CMOS は近い将来 600-GHz を超える
  CMOS will reach over 600-GHz in near future
  - Easy to access
  - But, limited performance of RF-power and noise figure
- アンテナの改善は必須
  Further improvement on antenna is necessary
  - Note that antenna has very long research history even in Terahertz region → technical limitation?
  - Share of system budget load with T/Rx

最後に

- 1-mW Output power in Tx
  - HBTs offer more than 1-mW output power at 324 GHz
  - It is still challenging work for many other devices (200~500-uW)
  - Faster devices → lower breakdown → lower output power
  - But, 1-mW looks not so far, if we can improve the efficiency just a little
- 15-dB Noise figure of Rx
  - HEMT amplifier with 7.5-dB NF at 270 GHz
  - Faster devices → higher gain at 300 GHz → lower NF
  - 5-dB or less NF is achievable ?!
- 25-dBi Antenna
  - Approximately 10~14-dB antenna gain with planar on-chip antenna.
  - It looks upper boundary, and even we need complicated technologies such as a micromachining or arrayed antenna
  - Packaging issue: horn-antenna, lens, and cavity
- **シグナルのロスの除去がテラヘルツデバイスではキーポイント !!!**

Dielectric Loss in Substrate

Substrate	ε_r	Tangental Loss
Silicon	12.0~12.7	0.02 @ 10 GHz
GaAs	13.0	0.0016 @ 10 GHz
Alumina	9.6~9.9	0.0003 @ 10 GHz
Fused Silica (Glass)	3.8	0.0002 @ 10 GHz
Fused Quartz	3.8	0.0001 @ 10 GHz